SA3086D

.

80 CH SEGMENT /COMMON DRIVER FOR DOT MATRIX LCD

Technical Specification

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Introduction

The SA3086D is an LCD driver LSI that is fabricated by low power CMOS high voltage process technology. Since this product can be used as segment or common driver, for LCD panel can be configured only with this product. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

Feature

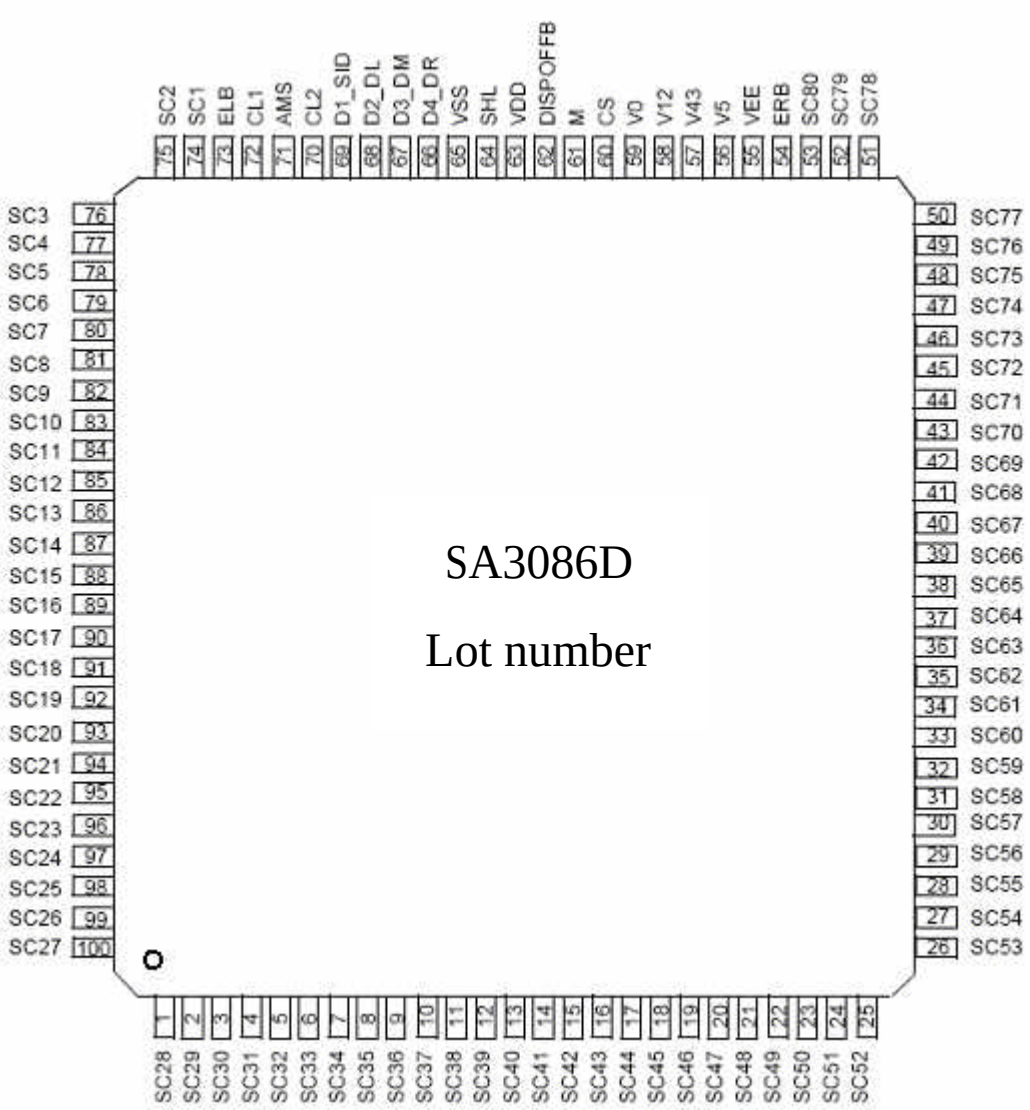
Power supply voltage	: 2.7 to 5.5V
LCD display voltage	: 6 to 28V (V_{DD}-V_{EE})
Segment mode	: 4 bit parallel / 1 bit serial
Common mode	: Single or dual mode operation
Display off function	: Power down function (in segment mode)
Display Duty	: Up to 1/240

DRIVERS	
COM (cascade)	SEG (cascade)
SA3086D	SA3086D

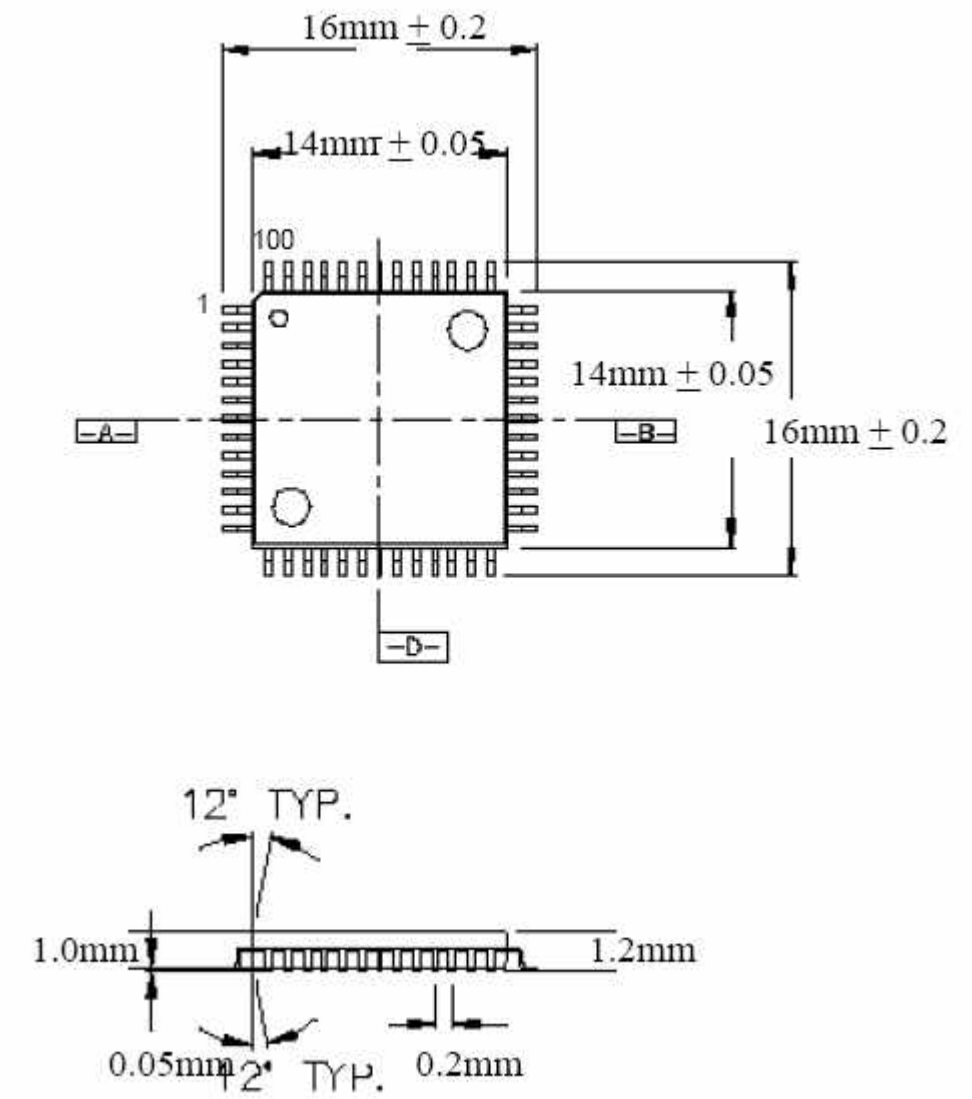
- High voltage CMOS process
- Bare die, TQFP, LQFP

Package Information

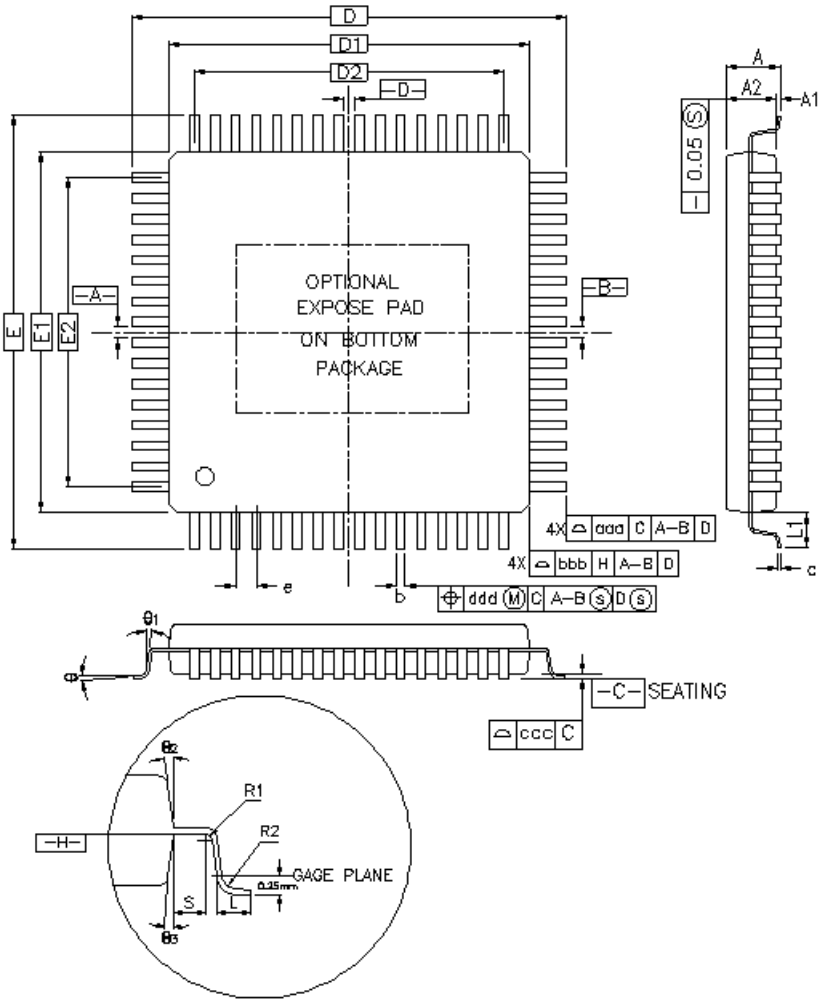
100 LEAD TQFP, LQFP



TQFP Package



LQFP Package



Note:

Option:

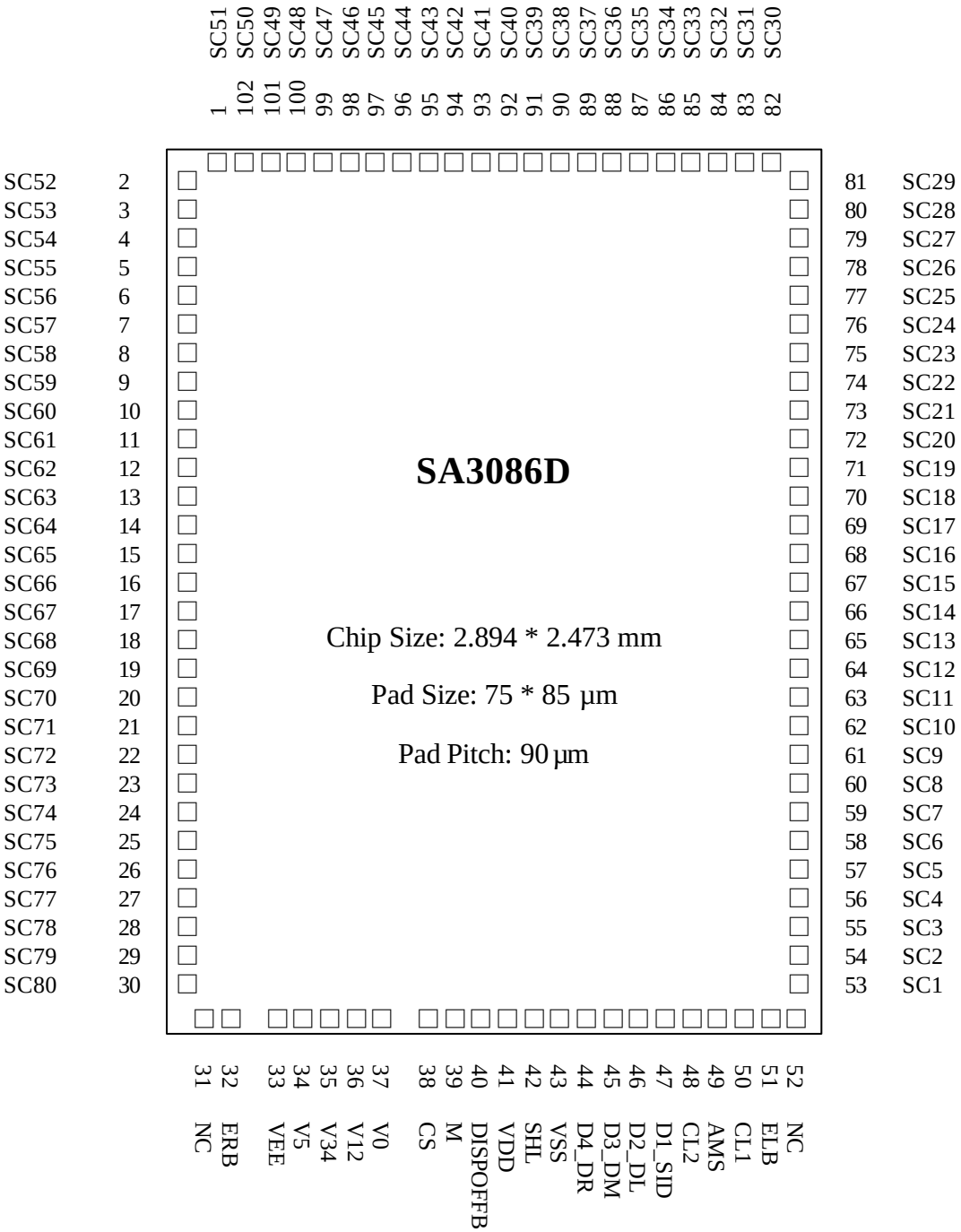
SQUARE DOTTED LINE IS E-PAD OUTLINE SIZE DEPENDENT ON DIE ATTACH PAD

Symbol	Millimeter			Inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.6D	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
D2	12.00			0.472		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
E2	12.00			0.472		
R2	0.08	-	0.20	0.003	-	0.008
R1	0.06	-	-	0.003	-	-
θ	0^o	3.5^o	7^o	0^o	3.5^o	7^o
θ1	0^o	-	-	0^o	-	-
θ2	11^o	12^o	13^o	11^o	12^o	13^o
θ3	11^o	12^o	13^o	11^o	12^o	13^o
c	0.09	-	0.20	0.004	-	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
	0.20	-	-	0.008	-	-

Notes:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMINSIONS INCLUDING MOLD MISMATCH
2. DIMINSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.

Pad Diagram



Die substrate should be connected to V_{DD}.

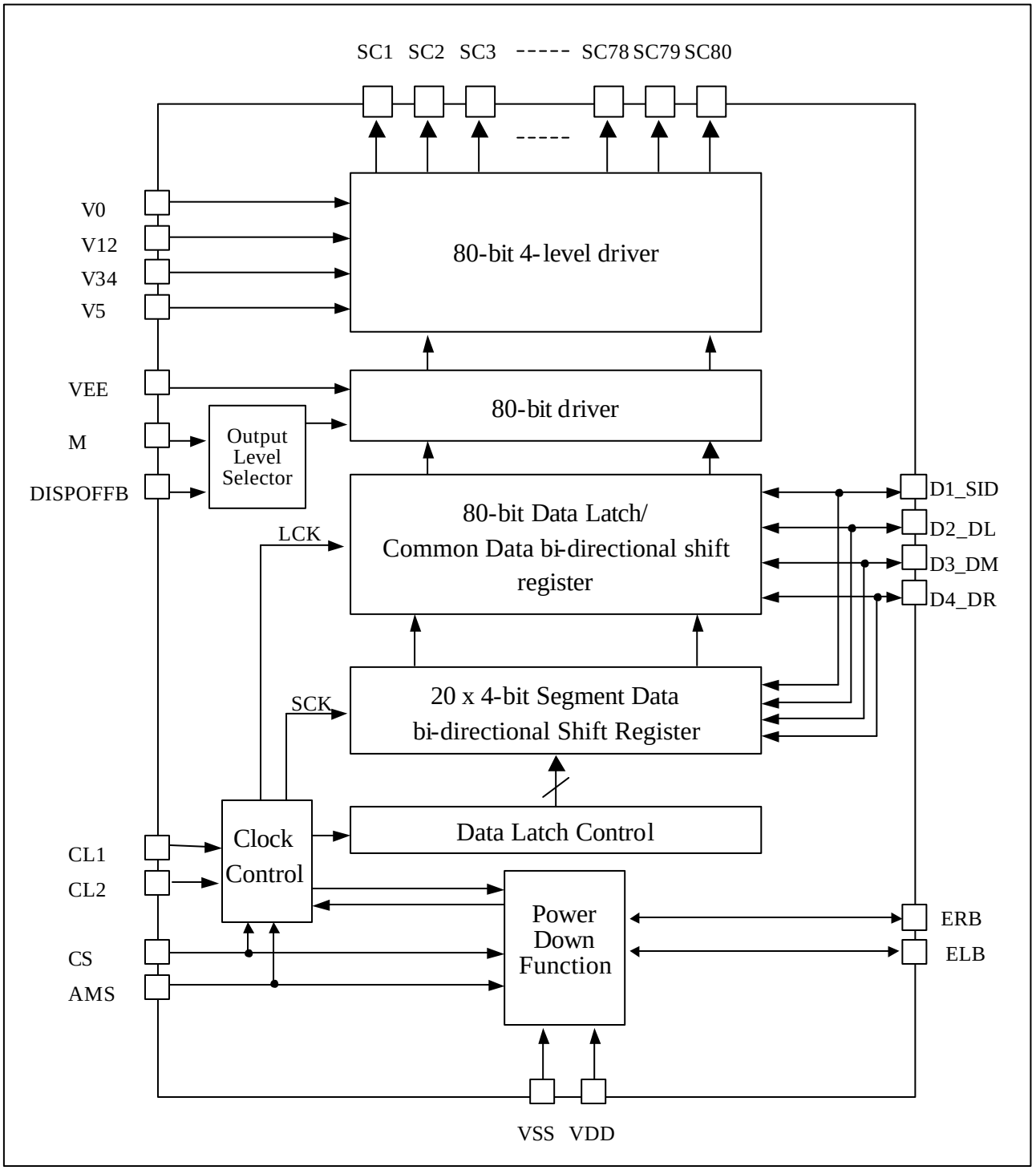
Please use the 1mil bonding line to bonding.

請使用 1mil 的邦定線作邦定。

Pad Location

No	Name	X	Y
1	SC51	316.6	2825.85
2	SC52	118.05	2712.65
3	SC53	118.05	2607.65
4	SC54	118.05	2502.65
5	SC55	118.05	2397.65
6	SC56	118.05	2307.65
7	SC57	118.05	2217.65
8	SC58	118.05	2127.65
9	SC59	118.05	2037.65
10	SC60	118.05	1947.65
11	SC61	118.05	1857.65
12	SC62	118.05	1767.65
13	SC63	118.05	1677.65
14	SC64	118.05	1587.65
15	SC65	118.05	1497.65
16	SC66	118.05	1407.65
17	SC67	118.05	1317.65
18	SC68	118.05	1227.65
19	SC69	118.05	1137.65
20	SC70	118.05	1047.65
21	SC71	118.05	957.65
22	SC72	118.05	867.65
23	SC73	118.05	777.65
24	SC74	118.05	687.65
25	SC75	118.05	597.65
26	SC76	118.05	507.65
27	SC77	118.05	417.65
28	SC78	118.05	312.65
29	SC79	118.05	207.65
30	SC80	118.05	102.65
31	NC	275.45	120.75
32	ERB	370.45	120.75
33	VEE	497.05	120.75
34	V5	587.05	120.75
35	V34	677.05	120.75
36	V12	767.05	120.75
37	V0	857.05	120.75
38	CS	982.75	120.75
39	M	1072.75	120.75
40	DISPOFFB	1162.75	120.75
41	VDD	1252.75	120.75
42	SHL	1342.75	120.75
43	VSS	1432.75	120.75
44	D4_DR	1522.75	120.75
45	D3_DM	1612.75	120.75
46	D2_DL	1702.75	120.75
47	D1_SID	1792.75	120.75
48	CL2	1882.75	120.75
49	AMS	1972.75	120.75
50	CL1	2062.75	120.75
51	ELB	2152.75	120.75
52	NC	2242.75	120.75
53	SC1	2405.15	102.65
54	SC2	2405.15	207.65
55	SC3	2405.15	312.65
56	SC4	2405.15	417.65
57	SC5	2405.15	507.65
58	SC6	2405.15	597.65
59	SC7	2405.15	687.65
60	SC8	2405.15	777.65
61	SC9	2405.15	867.65
62	SC10	2405.15	957.65
63	SC11	2405.15	1047.65
64	SC12	2405.15	1137.65
65	SC13	2405.15	1227.65
66	SC14	2405.15	1317.65
67	SC15	2405.15	1407.65
68	SC16	2405.15	1497.65
69	SC17	2405.15	1587.65
70	SC18	2405.15	1677.65
71	SC19	2405.15	1767.65
72	SC20	2405.15	1857.65
73	SC21	2405.15	1947.65
74	SC22	2405.15	2037.65
75	SC23	2405.15	2127.65
76	SC24	2405.15	2217.65
77	SC25	2405.15	2307.65
78	SC26	2405.15	2397.65
79	SC27	2405.15	2502.65
80	SC28	2405.15	2607.65
81	SC29	2405.15	2712.65
82	SC30	2206.60	2825.85
83	SC31	2116.60	2825.85
84	SC32	2026.60	2825.85
85	SC33	1936.60	2825.85
86	SC34	1846.60	2825.85
87	SC35	1756.60	2825.85
88	SC36	1666.60	2825.85
89	SC37	1576.60	2825.85
90	SC38	1486.60	2825.85
91	SC39	1396.60	2825.85
92	SC40	1306.60	2825.85
93	SC41	1216.60	2825.85
94	SC42	1126.60	2825.85
95	SC43	1036.60	2825.85
96	SC44	946.60	2825.85
97	SC45	856.60	2825.85
98	SC46	766.60	2825.85
99	SC47	676.60	2825.85
100	SC48	586.60	2825.85
101	SC49	496.60	2825.85
102	SC50	406.60	2825.85

Block Diagram



Block Description

Name	Function	COM/SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control timing according to the input of CL1, CL2 and control inputs (CS, AMS). In common driver application, this block generates shift clock (LCK) for the common data bidirectional shift register.	COM/SEG
Data latch control	Determines the direction of segment data shift, and input data of each bidirectional shift register. In case of 4-bit segment data parallel transfer mode, 4-bit unit shifts data. In case of common driver application mode, data is transferred to the common data shift register directly, so this block is not work.	SEG
Power down function	Controls the clocks enable state of current driver according to the input value of enable pin (ELB or ERB). If enable input value is ‘Low’, every clock of the current driver is enabled and the clock control block works. But if enable input is ‘High’, current driver is disabled and the input data value has no effect to the output level. So power consumption can be lowered.	SEG
Output level selector	Control the output voltage level according to the input control pin (M and DISPOFFB) (refer to Pin Description).	COM/SEG
80-bit data latch / common data bidirectional shift register	In segment driver application, the data from the 20x 4-bit segment data shift register are latched for segment driver output. When single-type common driver application, 1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. When dual-type common application mode, 80-bit two divides registers blocks and controlled independently (refer to NOTE 3).	COM/SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are logical voltage level and the outputs of this block are high voltage level value. And this value is input to the driver.	COM/SEG
80-bit 4-level driver	Selects the output voltage level according to the M and latched data value. If the data value is ‘High’ the driver output is selected voltage level (V0 or V5), and in the reverse case the driver output value is non-selected level (V12 or V34). In segment driver application, non-selected output value is V2 or V3. And when common driver application, this value becomes V1 or V4.	COM/SEG

Pin Description

<table>
<tr><th>Pin (No)</th><th>Input/ Output</th><th>Name</th><th>Description</th><th>Interface</th></tr>
<tr><td>VDD</td><td rowspan="3">Power</td><td rowspan="2">Operating Voltage</td><td>Logic power supply (2.7 to 5.5V)</td><td rowspan="3">Power</td></tr>
<tr><td>Vss</td><td>0V (GND)</td></tr>
<tr><td>VEE</td><td>Driver Supply Voltage</td><td>Power supply for driving the LCD</td></tr>
<tr><td>V0, V12, V34, V5</td><td>Input</td><td>LCD driver output voltage level</td><td>Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source (refer to NOTE 2).</td><td>Power</td></tr>
<tr><td>SC1 ~ SC80</td><td>Output</td><td>LCD driver output</td><td>Display data output pin, which corresponds to the respective latch contents. One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to NOTE 1).</td><td>LCD</td></tr>
<tr><td>CL1</td><td>Input</td><td>Data latch clock</td><td>• In segment application, CL1 is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse ‘High’ level initializes power-down function block.
• In common driver application, CL1 is used as shifting clock of common output data.</td><td>Controller</td></tr>
<tr><td>CL2</td><td>Input</td><td>Data shift clock</td><td>Clock pulse input for the bidirectional shift register.
• In segment application, CL2 is used as display data latch signal at the falling edge. This pulse, which was input when the enable bit (ELB/ERB) is not active condition, is invalid.
• In common application, the data is shifted to 80-bit common data bidirectional shift register by the CL1 clock.
So this clock pin need connect capacitor to VSS.</td><td>Controller</td></tr>
<tr><td>M</td><td>Input</td><td>Alternate signal for LCD driver output</td><td>Alternate signal input pin for LCD driving. Normal frame inversion signal is input to this pin.</td><td>Controller</td></tr>
<tr><td>DISPOFFB</td><td>Input</td><td>Display off control</td><td>Control input pin to fix the driver output (SC1~SC80) to V0 level, during ‘Low’ value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.</td><td>Controller</td></tr>
<tr><td>CS</td><td>Input</td><td>COM/SEG mode control</td><td>When CS = ‘Low’, SA3086D is used as 80-bit segment driver. When CS = ‘High’, SA3086D is set to 80-bit common driver.</td><td>VDD /Vss</td></tr>
<tr><td>AMS</td><td>Input</td><td>Application mode select</td><td>According to the input value of the AMS and the CS pin, application mode of SA3086D is different as below.
<table>
<tr><th>CS</th><th>AMS</th><th>Application mode</th><th>COM/SEG</th></tr>
<tr><td>L</td><td>L</td><td>4-bit parallel interface mode</td><td rowspan="2">SEG</td></tr>
<tr><td>L</td><td>H</td><td>1-bit serial interface mode</td></tr>
<tr><td>H</td><td>L</td><td>Single-type application mode</td><td rowspan="2">COM</td></tr>
<tr><td>H</td><td>H</td><td>Dual-type application mode</td></tr>
</table></td><td>VDD /Vss</td></tr>
</table>

Pin Description (continued)

<table>
<tr><th>Pin (No)</th><th>Input/ Output</th><th>Name</th><th>Function</th><th>Interface</th></tr>
<tr><td>D1_SID, D2_DL, D3_DM, D4_DR</td><td>Input / Output</td><td>Display data input serial input data / left, right data input / output</td><td>• In segment application, these pins are used as 4-bit data input pin (When parallel mode), or D1SID is used as serial data input pin and other pins are not used. (Open or connect this to VDD) (When serial mode).
• In common application, the data are shifted from D2DL (D4DR) to D4DR (D2DL), when single-type application mode (AMS = ‘ Low’). In dual-type application case, the data are shifted from D2DL and D3DM (D4DR and D3DM) to D4-DR (D2 DL). In each case the direction of data shift is determined by SHL input, (refer to NOTE 3, NOTE4)</td><td>Controller</td></tr>
<tr><td>SHL</td><td>Input</td><td>Shift direction control</td><td>When SHL = ‘ Low’ , data is shifted from left to right When SHL = ‘ High’ , the direction is reversed, (refer to NOTE 3)</td><td>VDD /Vss</td></tr>
<tr><td>ELB, ERB</td><td>Input / Output</td><td>Enable data input / output</td><td>• In segment application, only when enable input (ELB or ERB) is ‘ Low’ , the internal operation is enabled (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. (Refer to NOTE 4)
<table>
<tr><td rowspan="2">SHL</td><td colspan="2">SEGMENT DRIVER</td></tr>
<tr><td>ELB</td><td>ERB</td></tr>
<tr><td>L</td><td>Output
(Last open)</td><td>Input
(First Vss)</td></tr>
<tr><td>H</td><td>Input
(First Vss)</td><td>Output
(Last open)</td></tr>
</table>
• In common application, power down function is not used. (Open)</td><td>-</td></tr>
<tr><td>NC</td><td>-</td><td>Test pin</td><td>Test function. Not connection for use</td><td>-</td></tr>
</table>

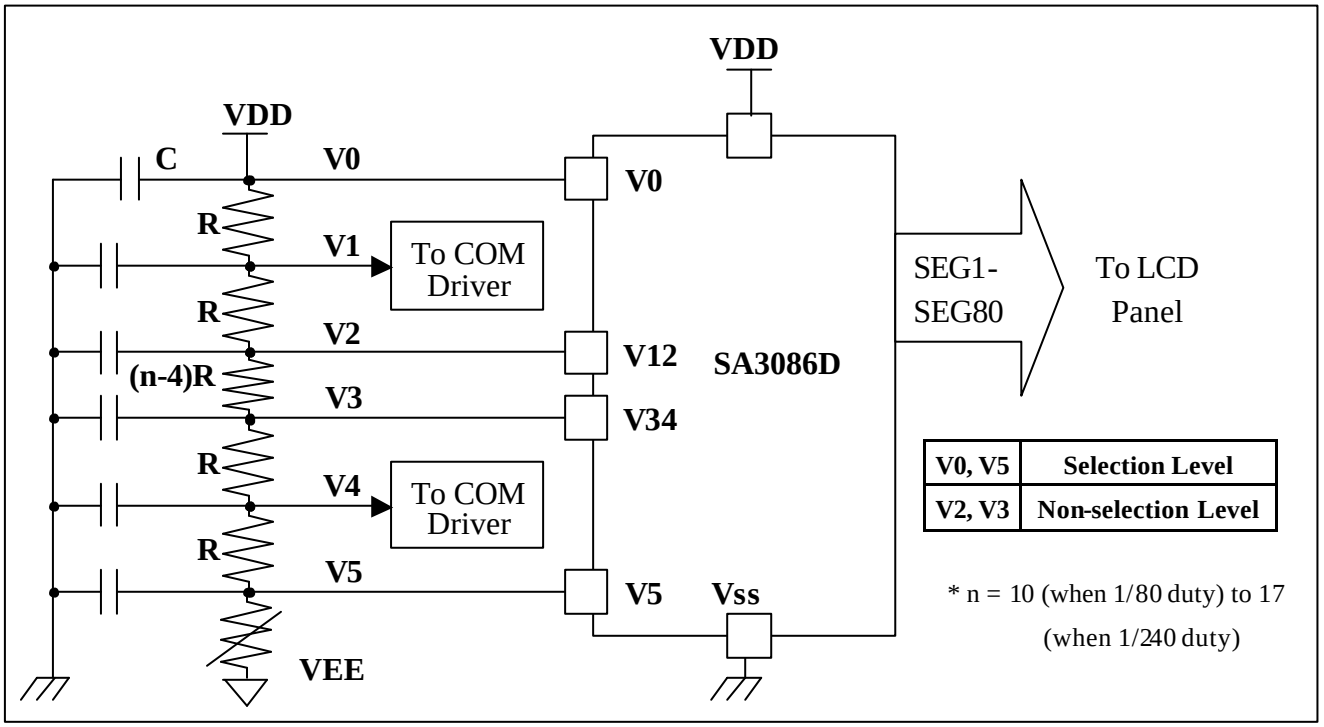
Note1. Output level control

X: Don't care

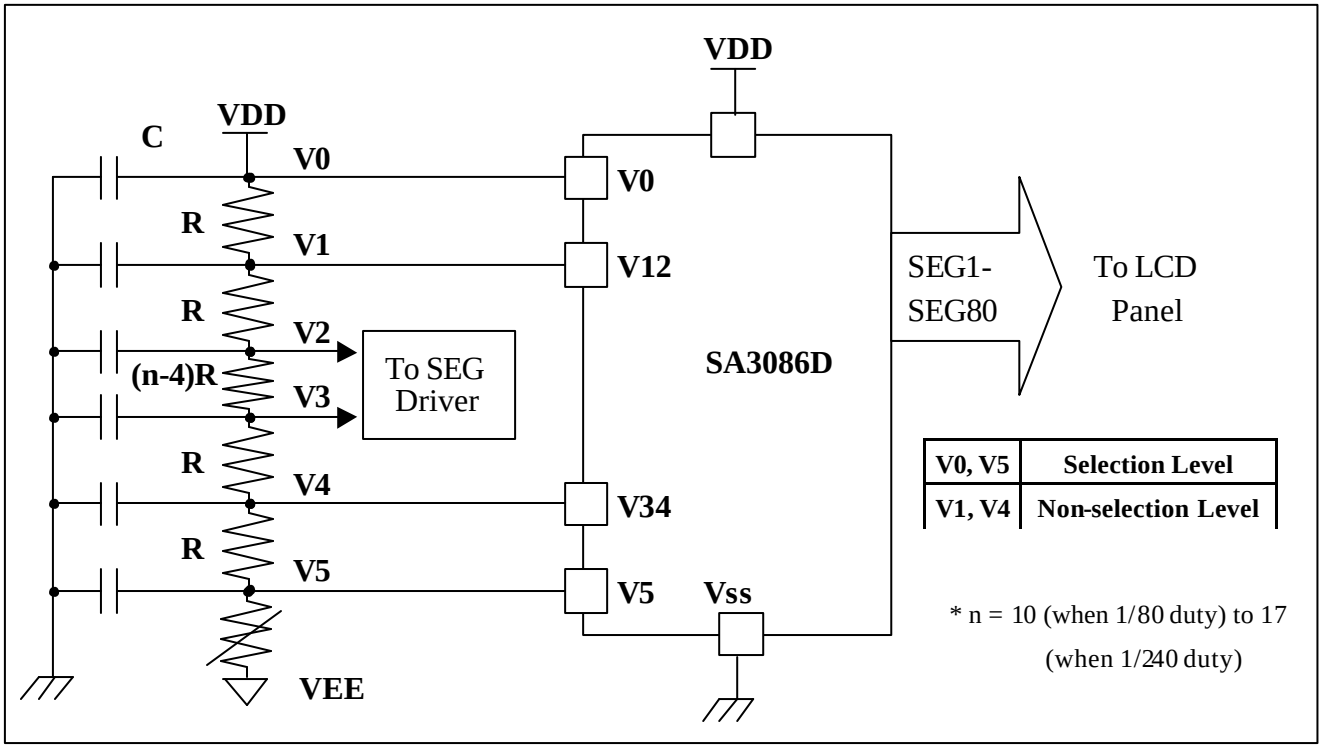
M	Latched data	DISPOFFB	Output level (SC1 ~ SC80)	
			SEG Mode	COM Mode
L	L	H	V12 (V2)	V12 (V1)
L	H	H	V0	V5
H	L	H	V34 (V3)	V34 (V4)
H	H	H	V5	V0
X	X	L	V0	V0

Note2. LCD Driving Voltage Application Circuit

(1) Segment driver application (CS = ‘ Low’)

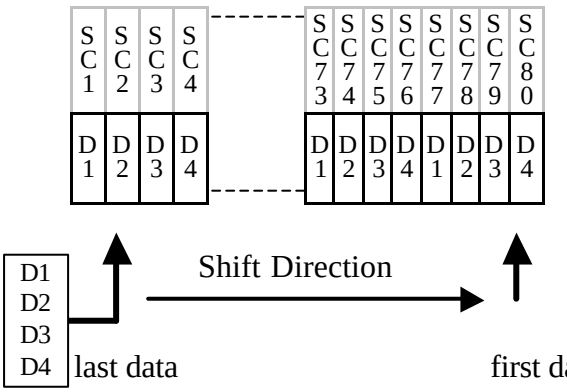
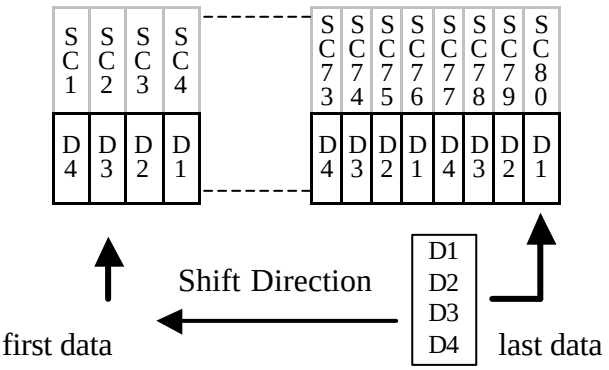
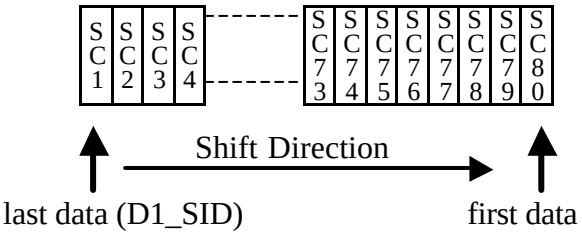
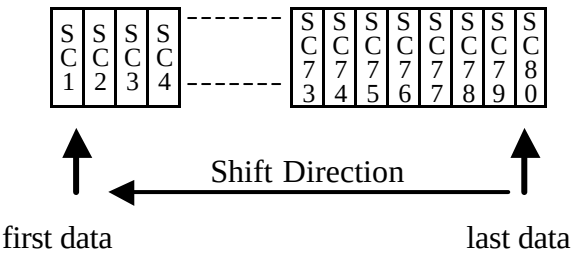


(2) Common driver application (CS = ‘ High’)

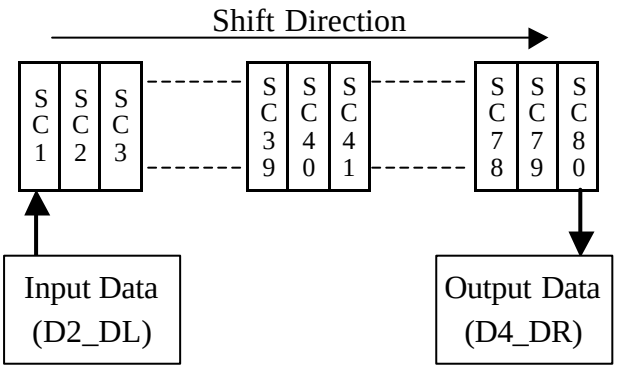
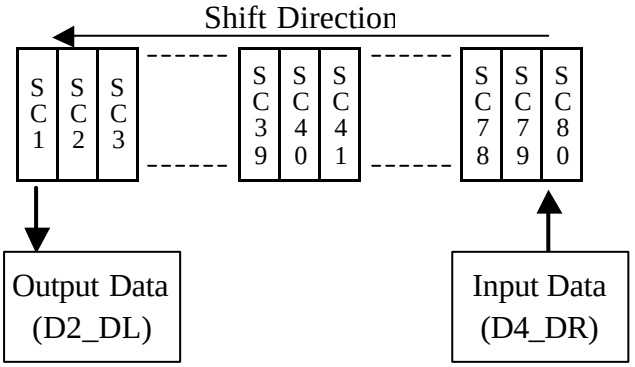
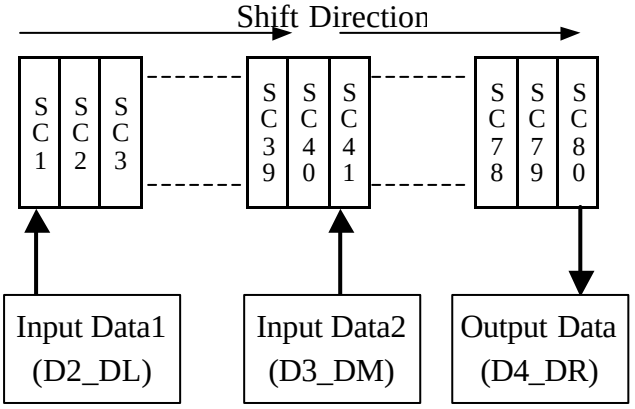
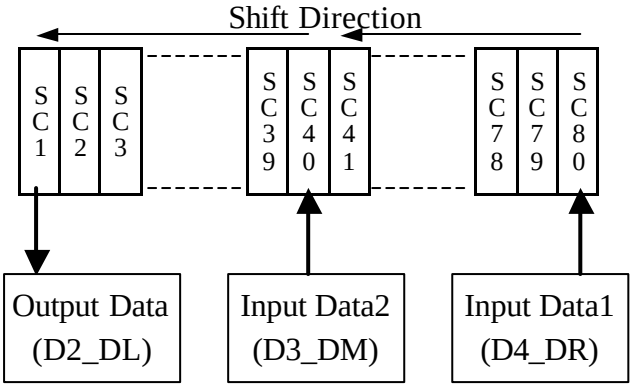


Note3. Data Shift Direction according to Control Signals

(1) When CS = ‘ Low’ (segment driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	4-Bit Parallel Data Transfer Mode (SEG)		D1_SID, D2_DL, D3_DM, D4_DR
	H			
H	L	1-Bit Serial Data Transfer Mode (SEG)		D1_SID
	H			

When CS = ‘ High’ (common driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	Single-type Application Mode (COM)		D2_DL
	H			D4_DR
H	L	Dual-type Application Mode (COM)		D2_DL, D3_DM
	H			D4_DR, D3_DM

Note4. Usage of Data Pins

COM /SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS = 'Low')	4 bit parallel interface mode (AMS = 'Low')	X	D1 (input)	D2 (input2)	D3 (input3)	D4 (input4)
	1 bit serial interface mode (AMS = 'Low')	X	SID (input)	Connect to VDD		
COM (CS = 'High')	Single type application mode (AMS = 'Low')	L	Open	DL (input)	Open	DR (output)
		H		DL (output)		DR (input)
	Dual type application mode (AMS = 'High')	L	Open	DL (input1)	DM (input2)	DR (output2)
		H		DL (output2)	DM (input2)	DR (input1)

Maximum Absolute Limit

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	-0.3 - +7.0	V
Driver supply voltage	V_{LCD}	0 - 30	
Input voltage	V_{IN}	-0.3 - V_{DD} +0.3	
Operating temperature	Topr	-30 - +85	℃
Storage temperature	Tstg	-55 - +150	

* **Note:** Voltage greater than above may do damage to the circuit.

Electrical Characteristics

DC Characteristics

(1) Segment Driver Application

(Vss = 0V, Ta = -30 to +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating Voltage 1	V_{DD}	-		2.7	-	5.5	V
	V_{LCD}	$V_{IN} = V_{DD} - V_{EE}$		6	-	28	
Input voltage (1)	V_{IH}	-		$0.8V_{DD}$	-	V_{DD}	
	V_{IL}	-		0	-	$0.2V_{DD}$	
Output voltage (2)	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	$V_{IN} = V_{DD}$ to V_{SS}		-10	-	10	µA
Input leakage current 2 (3)	I_{IL2}	$V_{IN} = V_{DD}$ to V_{EE}		-25	-	25	
On resistance (4)	R_{ON}	I_{ON} = 100µA		-	2	4	kΩ
Supply current (5)	I_{STBY}	f_{CL1} = 0Hz, M = Vss	Vss pin	-	-	6	µA
	I_{DD}	f_{CL1} = 32kHz, f_M = 80 Hz	V_{DD} = 5V	-	-	5	mA
			V_{DD} = 3V	-	-	2	
	I_{EE}		V_{DD} = 5V	-	-	500	µA

Notes:

1. Applied to CL1, CL2, ELB, ERB, D1_SID – D4_DR, SHL, DISPOFFB, M, CS, AMS pin
2. ELB, ERB pin
3. V0, V12, V43, V5 pin
4. $V_{LCD} = V_{DD} - V_{EE}$, V0 = V_{DD} = 5V, V5 = V_{EE} = -23 V
   V12 = V_{DD}-2/n (V_{LCD}), V43 = V_{EE}+2/n (V_{LCD}), n = 17 (1/240 duty, 1/17 bias)
5. V0 = V_{DD}, V12 = 1.71V(V_{DD} = 5V) or -0.06V (V_{DD} = 3V),
   V43=-19.71V (V_{DD}=5V) or -19.94V (V_{DD}=3V), V5=V_{EE} =-23V, no-load condition (1/240 duty, 1/17 bias)
   4-bit parallel interface mode
   I_{STBY}: V_{DD} = 5V, f_{CL2} = 0Hz, SHL = V_{SS}, DISPOFFB = V_{SS}, M = V_{SS}, display data pattern = 0000
   I_{DD}: V_{DD} = 3V, f_{CL2} = 4MHz, display data pattern = 0101, DISPOFFB = V_{DD}
   V_{DD} = 5 V, f_{CL2} = 5.12MHz, display data pattern = 0101, DISPOFFB = V_{DD}
   I_{EE}: V_{DD} = 5V, f_{CL2} = 5.12MHz, display data pattern = 0101, V_{EE} pin, DISPOFFB = V_{DD}

DC Characteristic (Continued)

(2) Common Driver Application

(Vss = 0V, Ta = -30 to +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating voltage1	V_{DD}	-		2.7	-	5.5	V
	V_{LCD}	$V_{IN} = V_{DD} - V_{EE}$		6	-	28	
Input voltage (1)	V_{IH}	-		$0.8V_{DD}$	-	V_{DD}	
	V_{IL}	-		0	-	$0.2V_{DD}$	
Output voltage (3)	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	$V_{IN} = V_{DD}$ to V_{SS}		-10	-	10	µA
Input leakage current 2 (2)	I_{IL2}	V_{IN} = 0V, V_{DD} = 5V (Pull Up)		-50	-125	-250	
Input leakage current 3 (4)	I_{IL3}	$V_{IN} = V_{DD}$ to V_{SS}		-25	-	25	
On resistance (5)	R_{ON}	I_{ON} = 100µA		-	2	4	kΩ
Supply current (6)	I_{STBY}	f_{CL1} = 0Hz	Vss pin	-	-	6	µA
	I_{DD}	f_{CL1} = 32kHz, f_M = 80 Hz	V_{DD} = 5V	-	-	200	
			V_{DD} = 3V	-	-	120	
	I_{EE}		V_{DD} = 5V	-	-	150	

Notes:

1. Applied to CL1, D2_DL (SHL = LOW), D4_DR (SHL = HIGH), SHL, DISPOFFB, M, CS, AMS pin
2. Pull-up input pins: CL2, D1_SID, D3_DM (AMS = HIGH), ELB (SHL = LOW), ERB (SHL = HIGH)
3. D2_DL (SHL = HIGH), D4_DR (SHL = LOW) pin
4. V0, V12, V43, V5 pin
5. $V_{KCD} = V_{DD}$-V_{EE}, V0 = V_{DD} = 5V, V5 = V_{EE} = -23V
   V12 = V_{DD}-1/n (V_{LCD}), V43 = V_{EE}+1/n(V_{LCD}), n = 17(1/240 duty, 1/17 bias)
6. V0 = V_{DD}, V12 = 3.35V (V_{DD} = 5V) or 1.47V (V_{DD} = 3V),
   V43=-21.35V (V_{DD}=5V) or-21.47V (V_{DD}=3V), V5=V_{EE}=-23V, no-load condition (1/240 duty, 1/17 bias)
   Single-type mode operation: AMS = V_{SS}, SHL = V_{SS}
   D1_SID = D3_DM = V_{DD}, D4_DR = OPEN, ELB = ERB = OPEN,
   I_{STBY}: V_{DD} = 5V, M = V_{SS}, D2_DL = V_{SS}, DISOFFB = V_{SS}
   I_{DD}: f_M = 80Hz, D2_DL = V_{DD}, , DISPOFFB = V_{DD}
   V_{DD} = 3 V, display data pattern = 10000000… , 01000000… , 00100000… , 00010000… , …
   V_{DD} = 5 V, display data pattern = 10000000… , 01000000… , 00100000… , 00010000… , …
   I_{EE}: f_M = 80Hz, D2_DL = V_{DD}, , DISPOFFB = V_{DD}
   V_{DD} = 5V, current through V_{EE} Pin, display data pattern = 10000000… , 01000000… , 00100000… , 00010000…

AC Characteristics

(1) Segment Driver Application

(V_{SS} = 0V, Ta = -30 to +85°C)

Characteristic	Symbol	Test Condition	(1) V_{DD} = 5V ± 10%			(2) V_{DD} = 3V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	125	-	-	250	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	-	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	t_{CS}	-	80	-	-	120	-	-	
Clock hold time	t_{CH}	-	80	-	-	120	-	-	
Propagation delay time	t_{PHL}	ELB Output	-	-	60	-	-	125	
		ERB Output			60			125	
ELB, ERB set-up time	t_{PUS}	ELB Input	30	-	-	65	-	-	
		ERB Input	30			65			
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-		ns
M – OUT propagation delay time	t_{PD1}	C_L = 15pF	-	-	1.0	-	-	1.2	µs
CL1 – OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t_{PD3}		-	-	1.0	-	-	1.2	

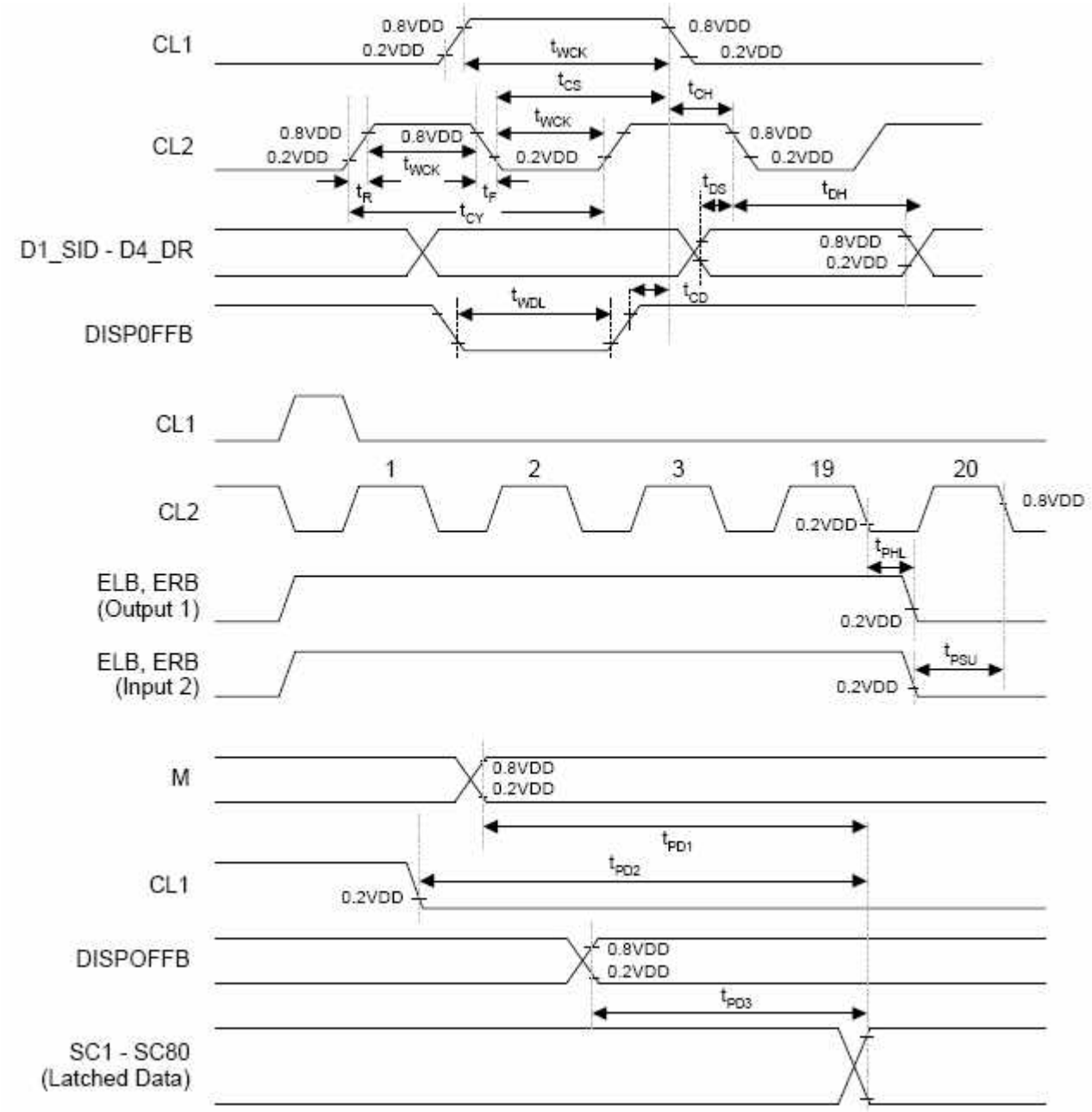
(2) Common Driver Application

(V_{SS} = 0V, Ta = - 30 to +85°C)

Characteristic	Symbol	Test Condition	(1) V_{DD} = 5V ± 10%			(2) V_{DD} = 3V ± 10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	t_{CY}	Duty = 50%	250	-	-	500	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	95	-	-	
Clock rise / fall time	t_R/t_F	-	-	-	50	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	100	-		ns
Output delay time	t_{DL}	C_L = 15pF	-	-	200	-	-	250	
M – OUT propagation delay time	t_{PD1}		-	-	1.0			1.2	µs
CL1 – OUT propagation delay time	t_{PD2}		-	-	1.0	-	-	1.2	
DISPOFFB – OUT propagation delay time	t_{PD3}				1.0			1.2	

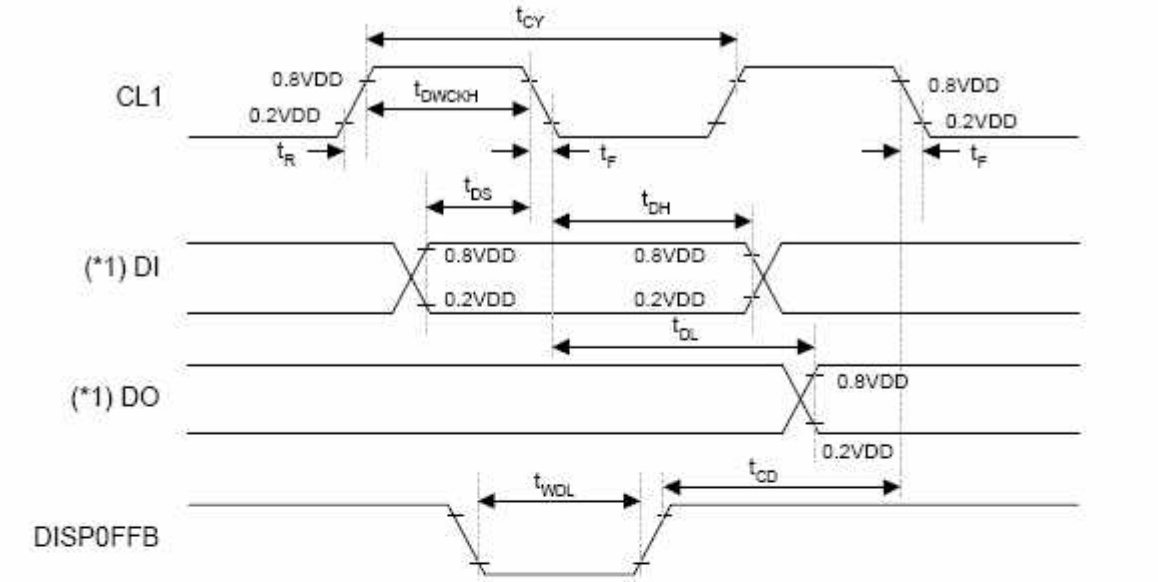
AC Characteristics (Continued)

(3) Segment Driver Application Timing

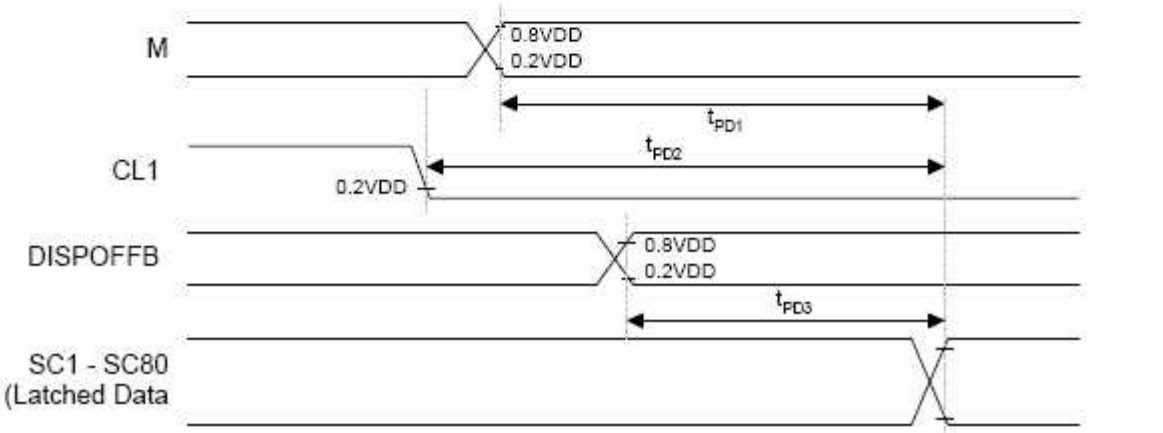


AC Characteristics (Continued)

(4) Common Driver Application Timing



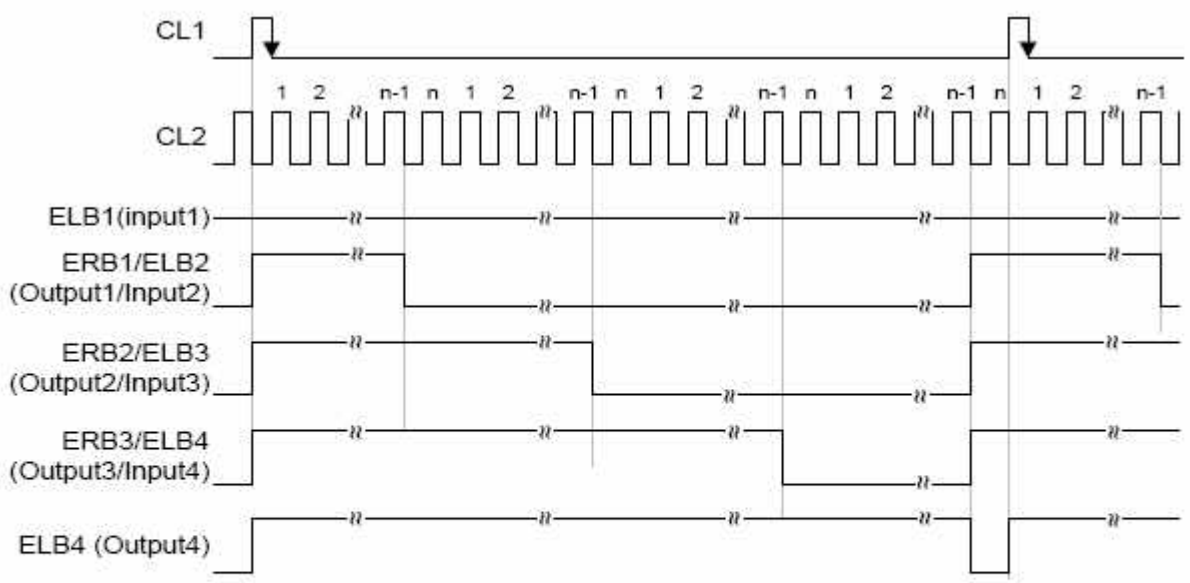
(*1) When in single-type interface mode
DI => D2_DL (SHL = L), D4_DR (SHL = H)
DO => D4_DR (SHL = L), D2_DL (SHL = H)
When in dual-type interface mode
DI => D2_DL and D3_DM (SHL = L), D4_DR and D3_DM (SHL = H)
DO => D4_DR (SHL = L), D2_DL (SHL = H)



Power Down Function

In the case of cascade connection of segment mode drivers, SA3086D has a ‘power down function’ in order to reduce the power consumption.

SHL	Enable input	Enable output	Current driver status	The other drivers status
L	ERB	ELB	While ERB = ‘Low’, current driver is enabled.	Disabled
H	ELB	ERB	While ELB = ‘Low’, current driver is enabled.	Disabled



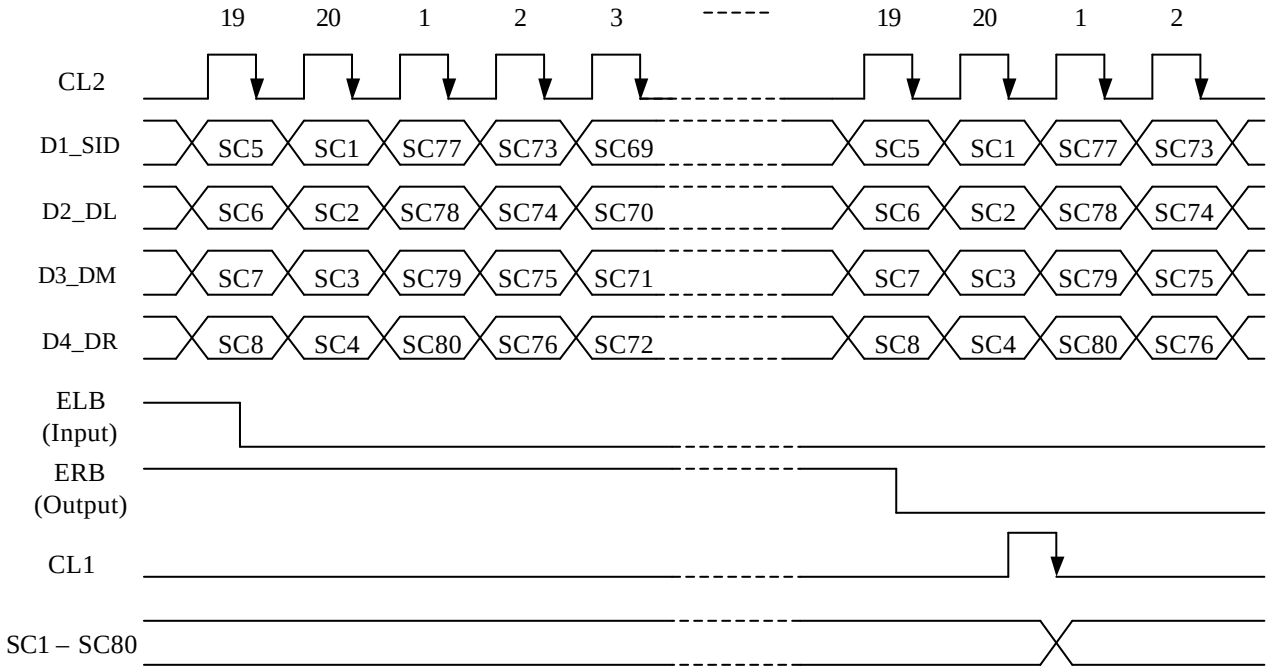
NOTES:

1. SHL = High (EBL = Input, ERB = Output)
   Current SA3086's ERB must be connected to the next SA3086's ELB.
2. When in 4-bit parallel interface mode: n = 20
   When in 1-bit serial interface mode: n = 80

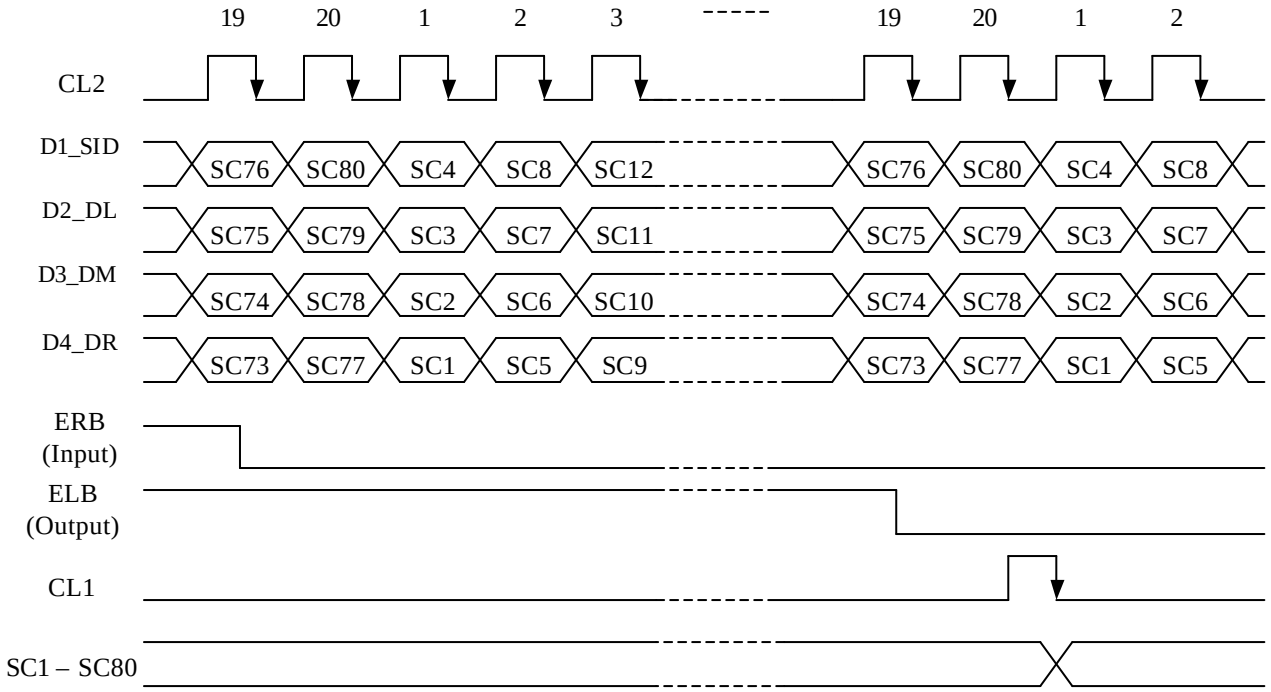
Operation Timing Diagram

(1) 4-BIT Parallel Mode Interface Segment Driver

- When SHL = ‘ Low’

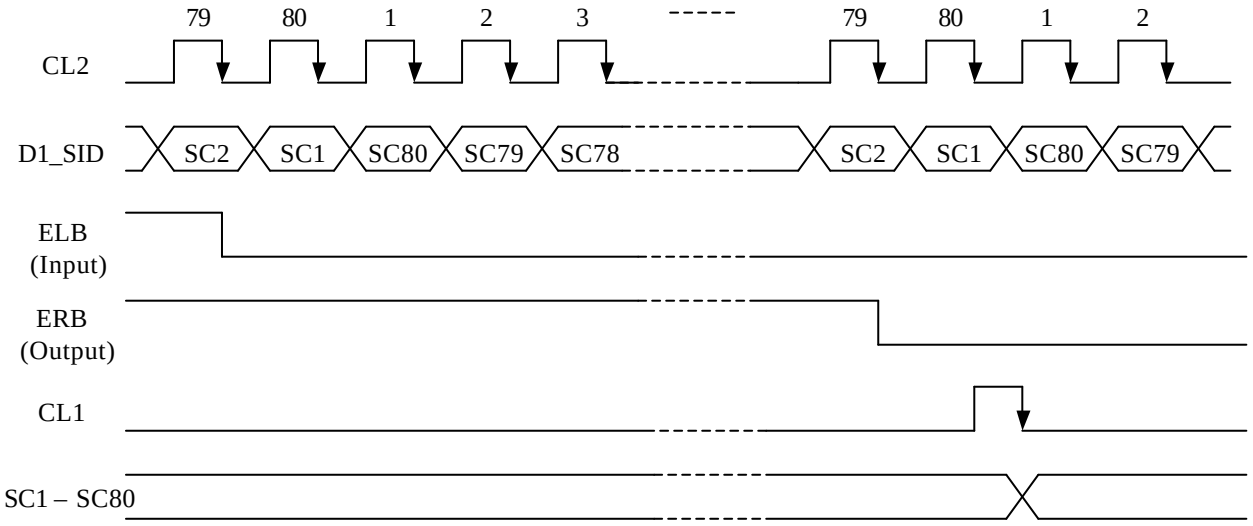


- When SHL = ‘ High’

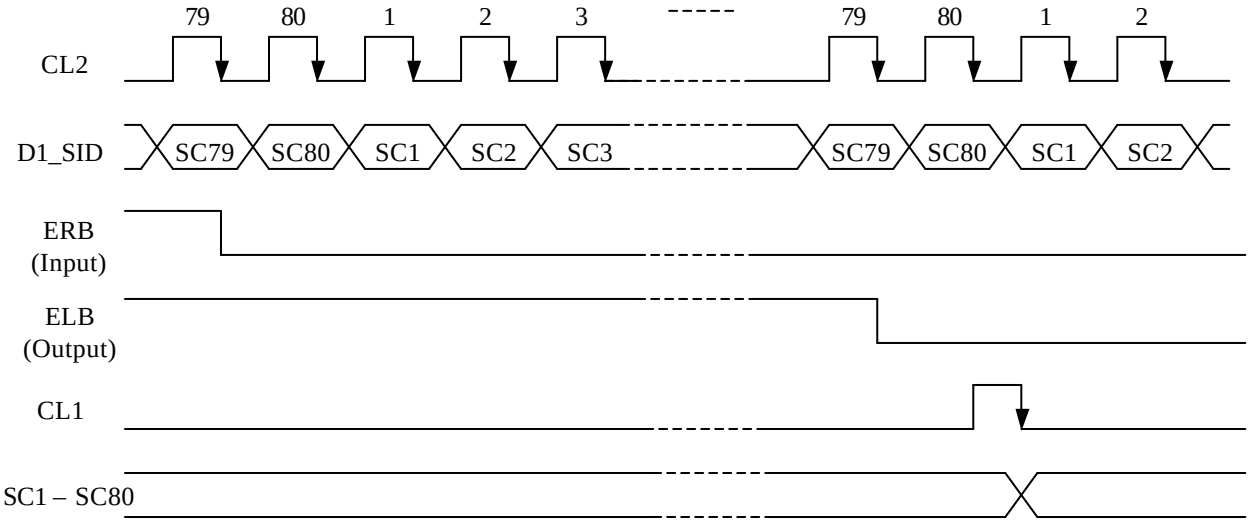


(2) 1-bit Serial Mode Interface Segment Driver

- When SHL = ‘ Low’

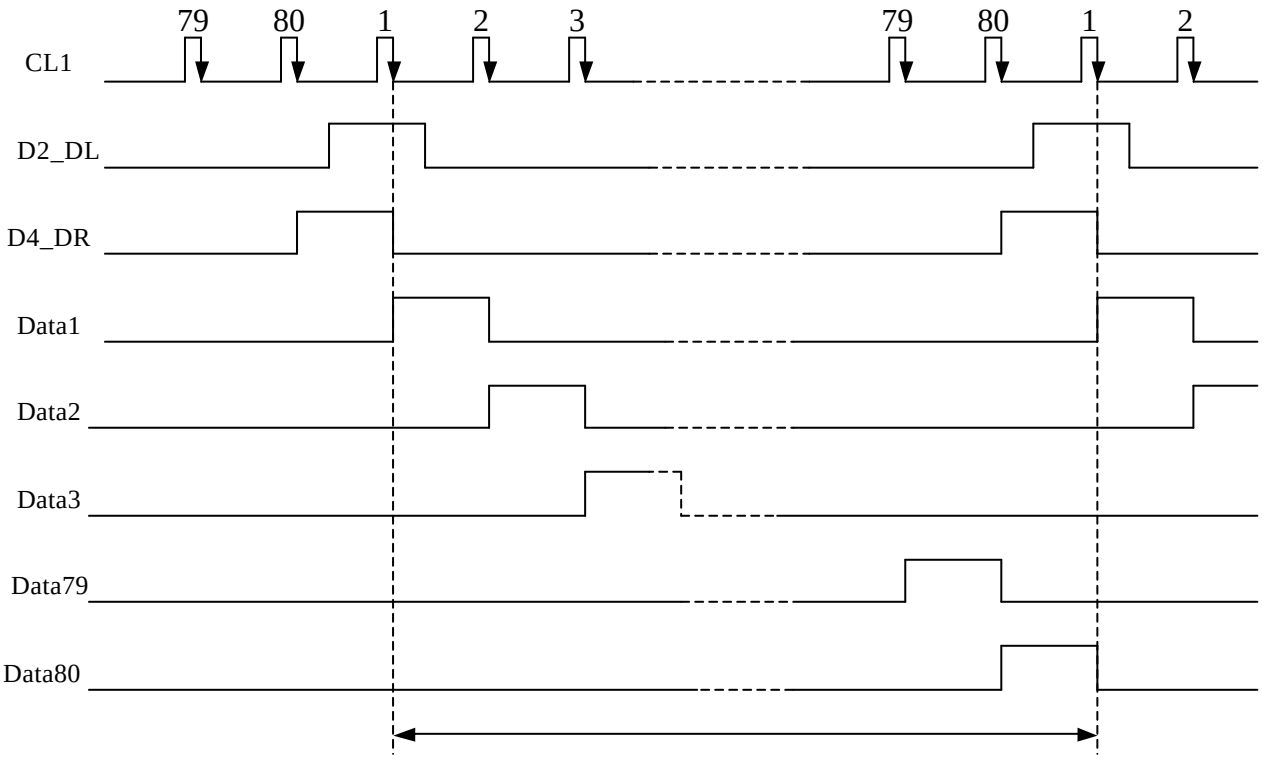


- When SHL = ‘ High’

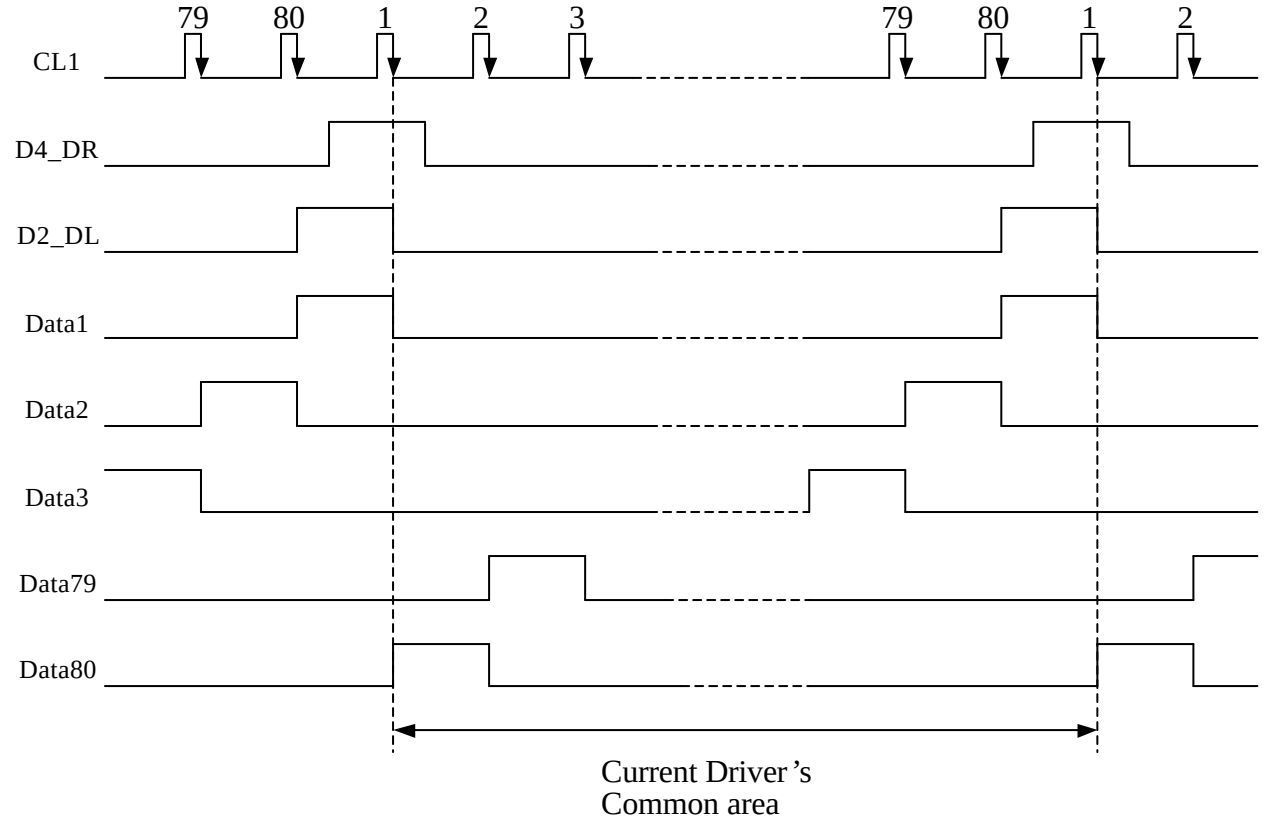


(3) Single-type Interface Mode Common Driver

- When SHL = ‘ Low’

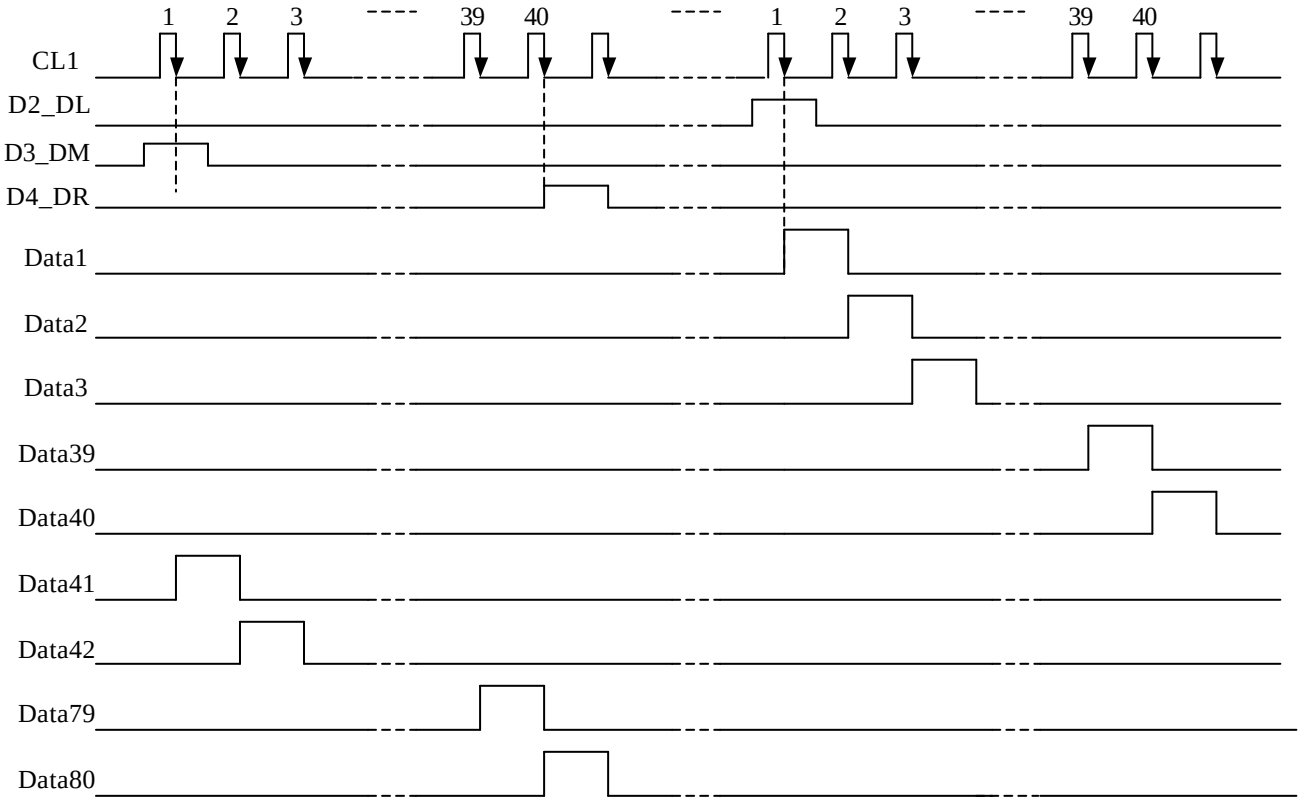


- When SHL = ‘ High’

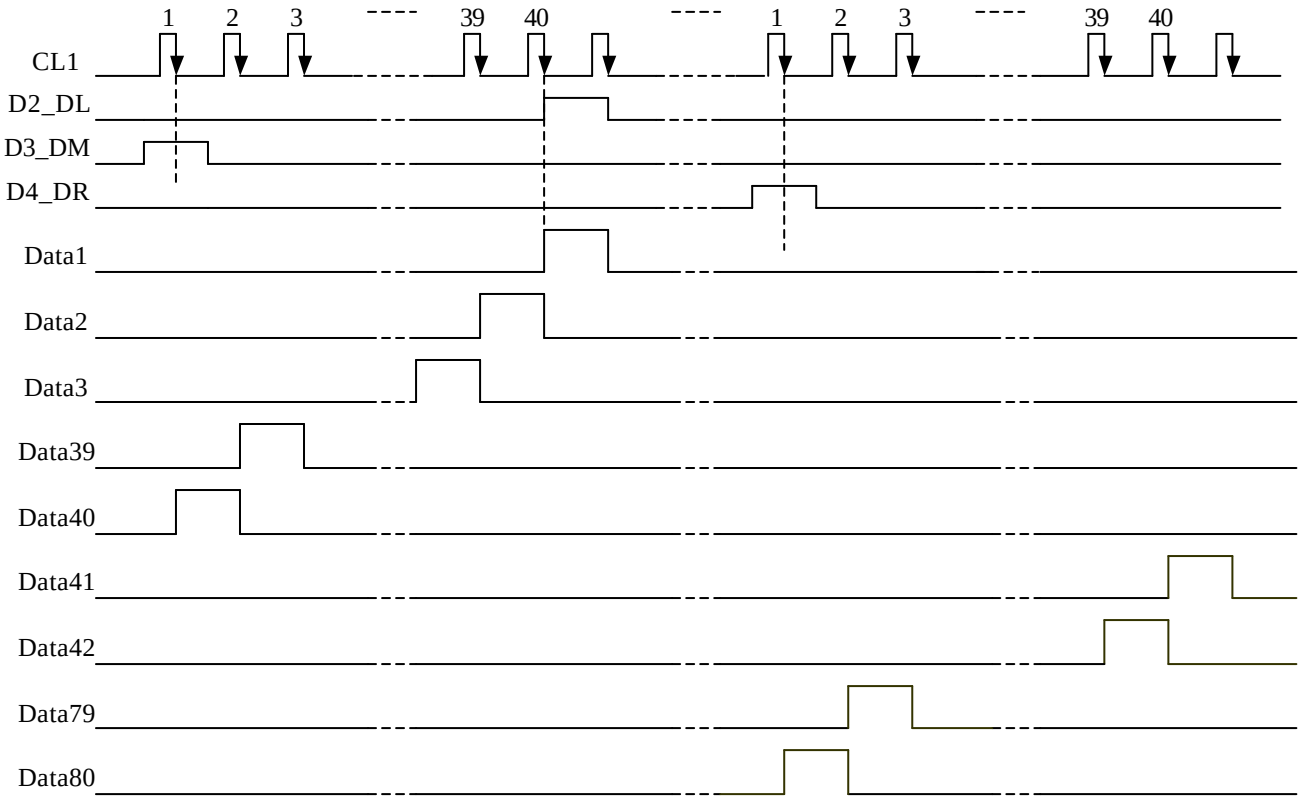


(4) Dual type interface mode driver

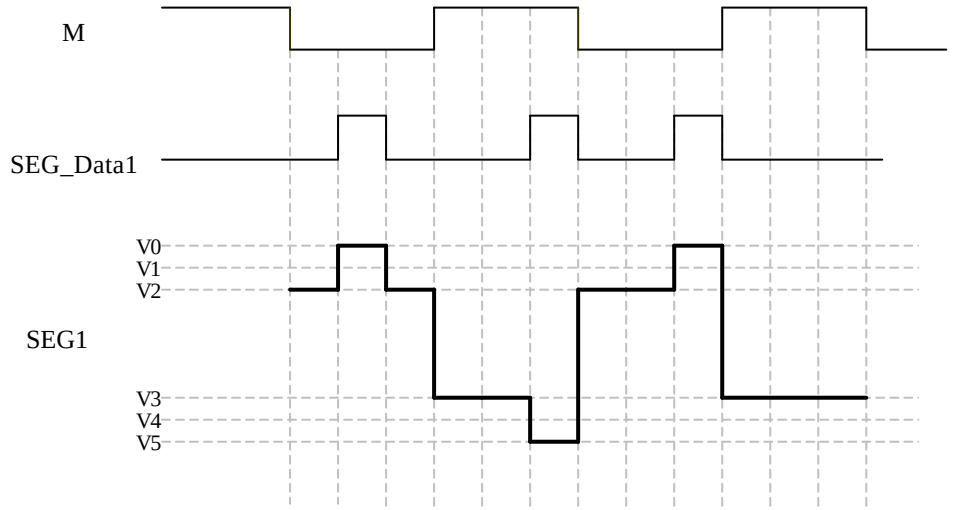
- When SHL = ‘ Low’



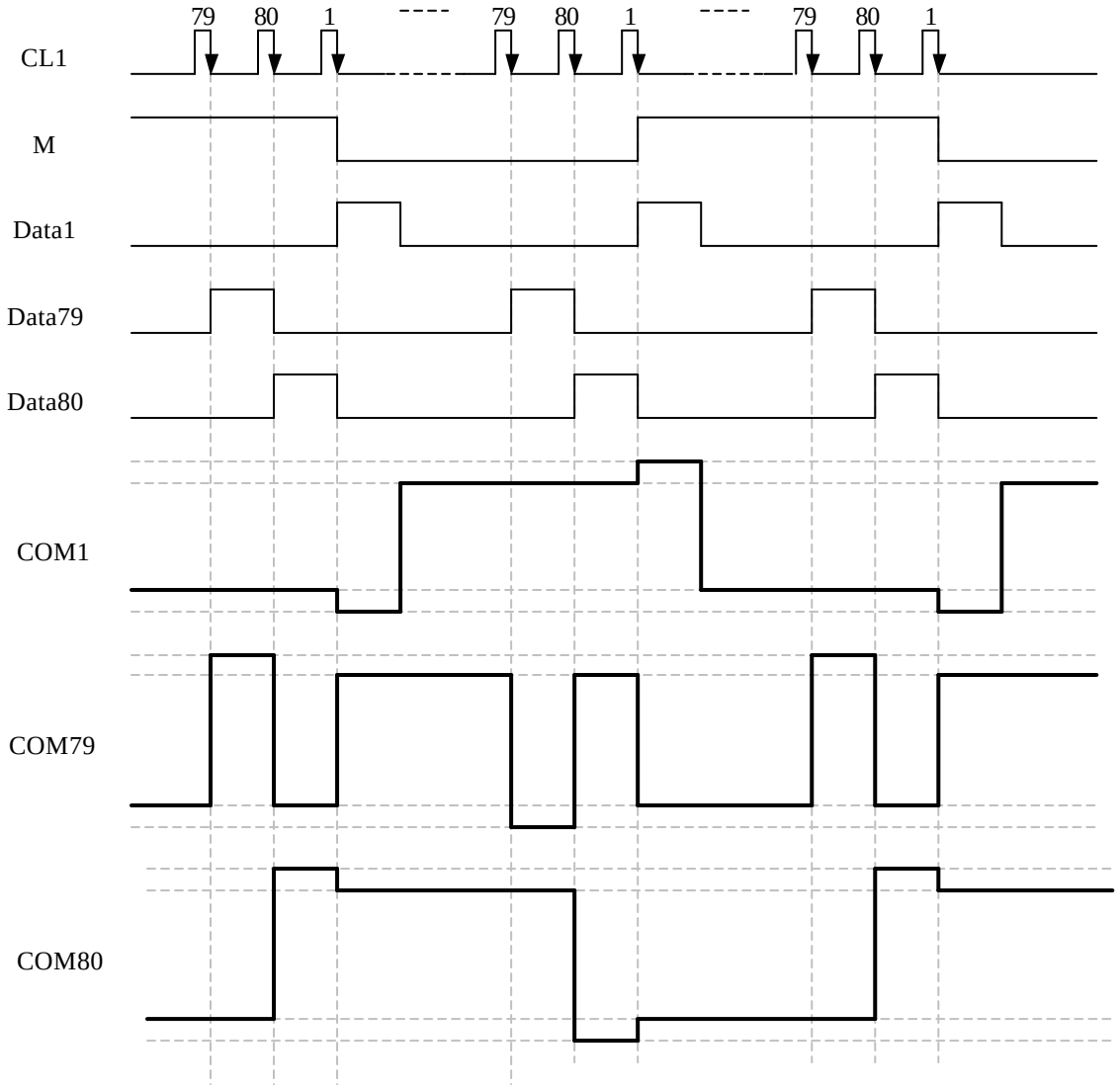
- When SHL = ‘ High’



(5) Segment Driver Timing



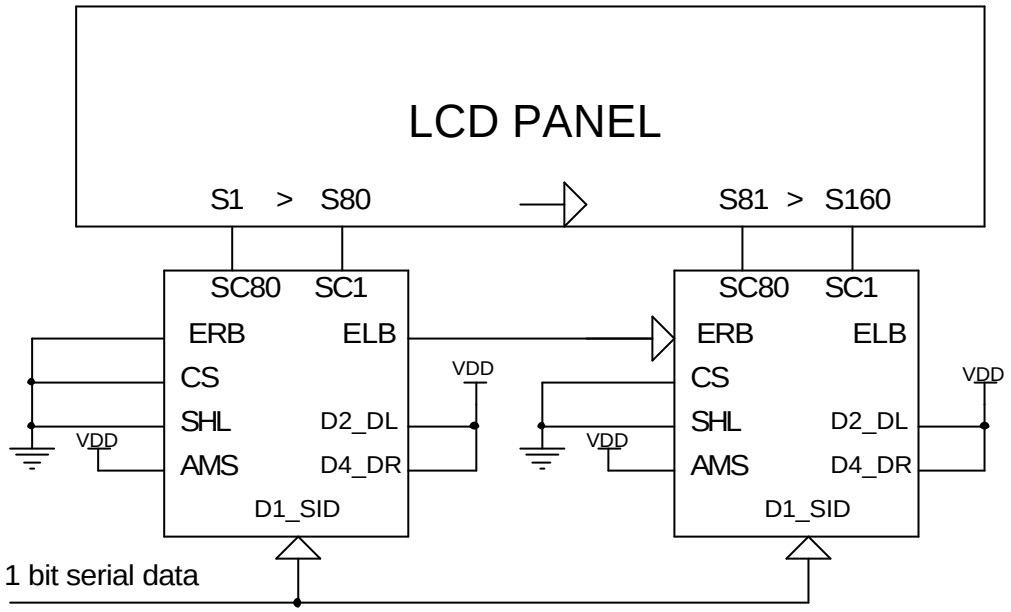
(6) Common Driver Timing



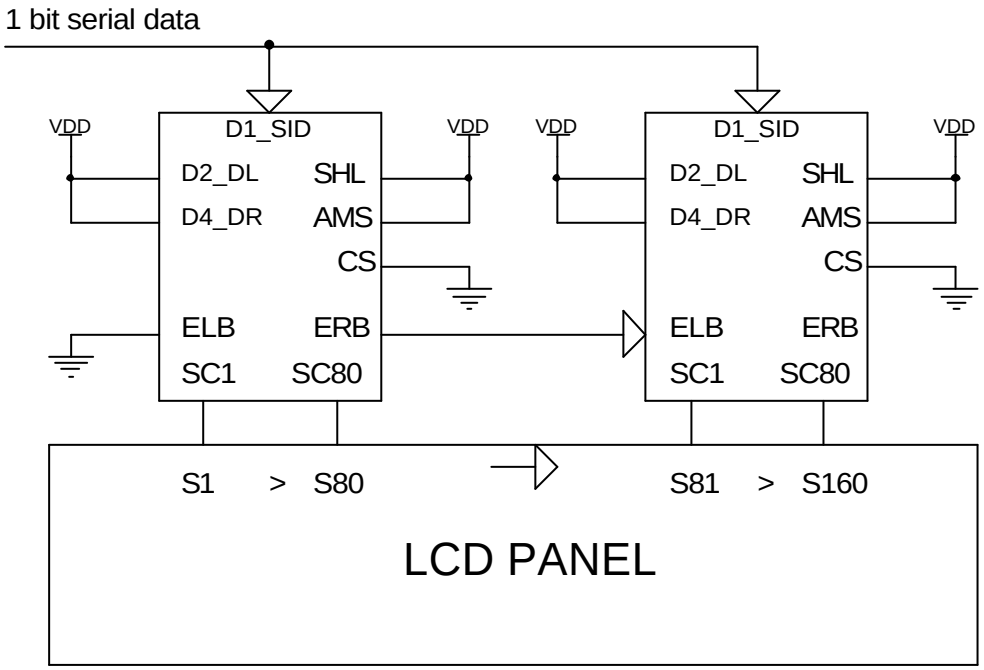
Application Information

1-bit Serial Interface (80-Ch. Segment Driver)

a) Lower View (SHL = L, AMS = H)

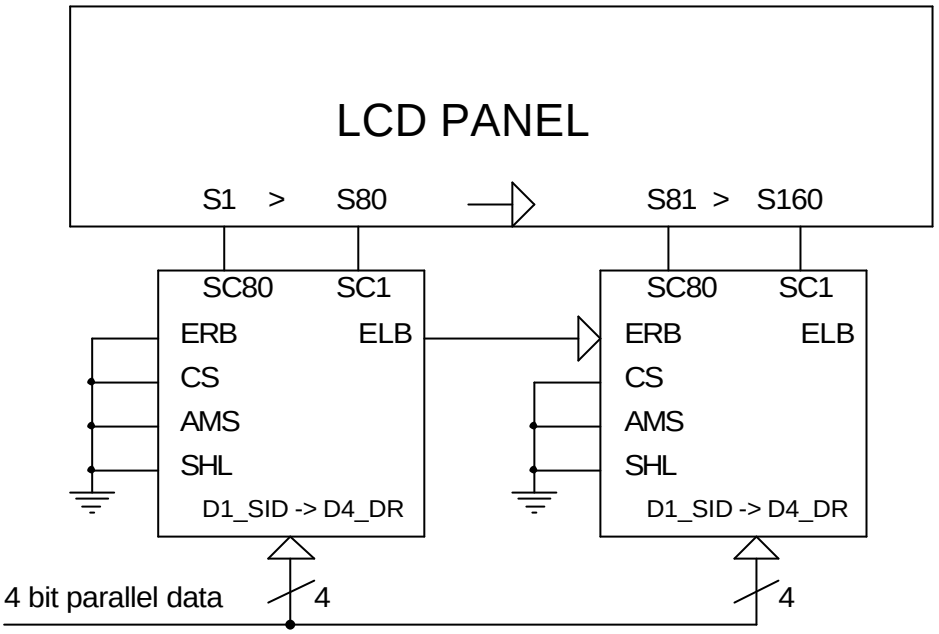


b) Upper View (SHL = H, AMS = H)

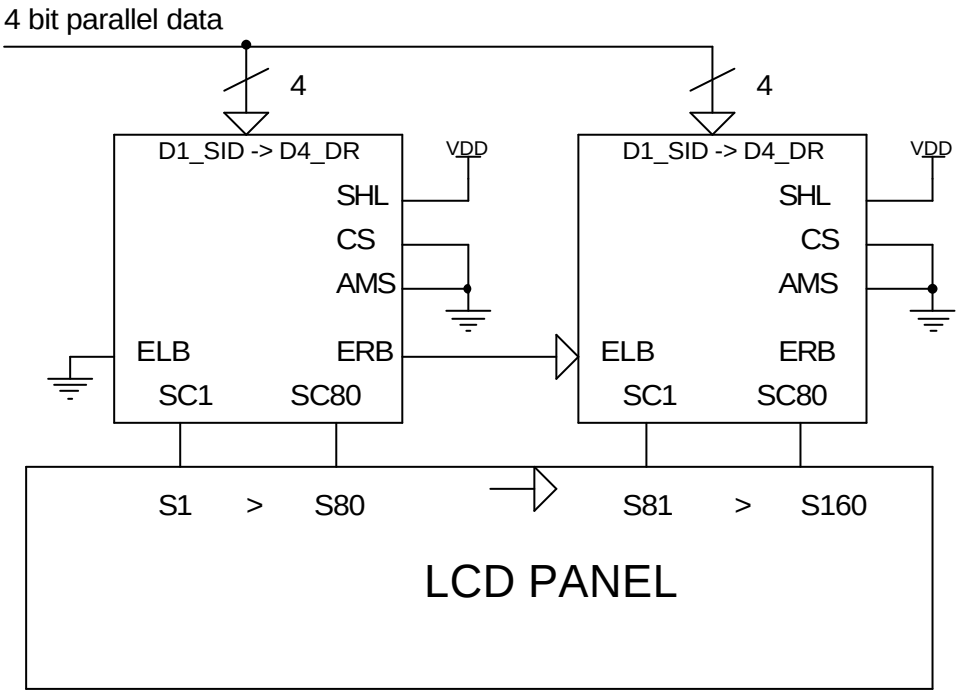


4-Bit Parallel Interface Mode (80 Ch. Segment Driver)

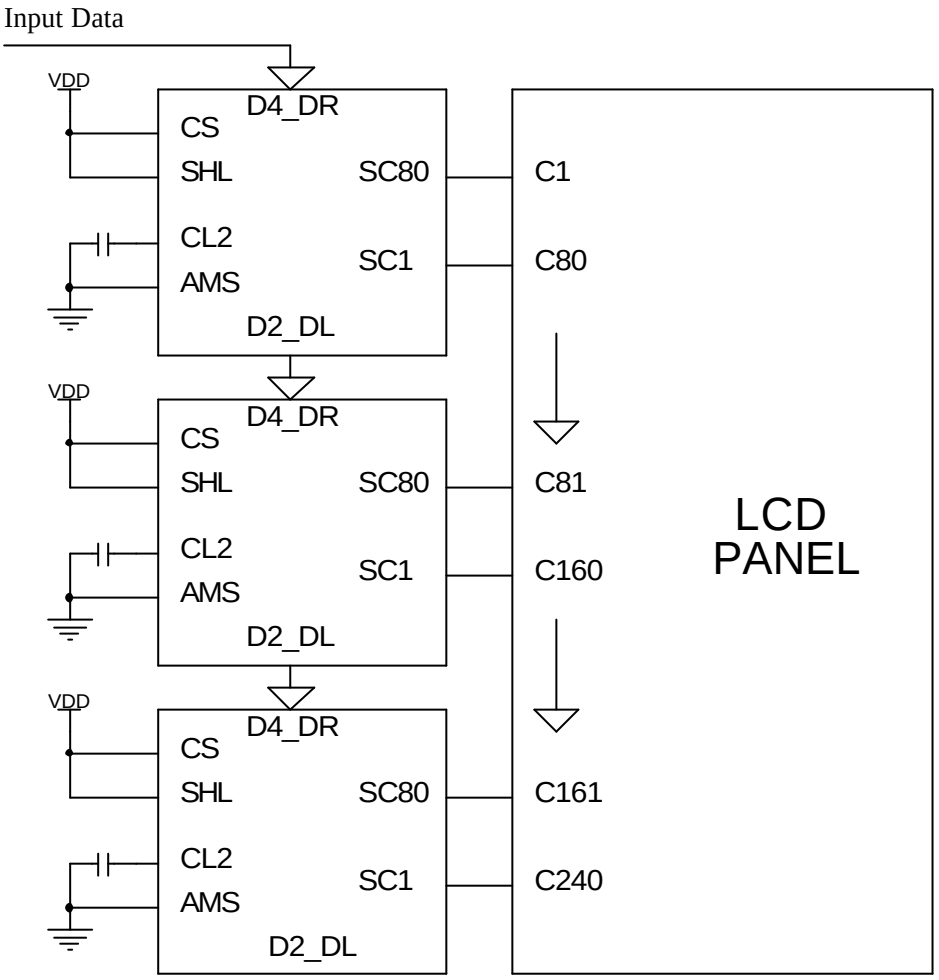
a) Lower View (SHL = L, AMS = L)



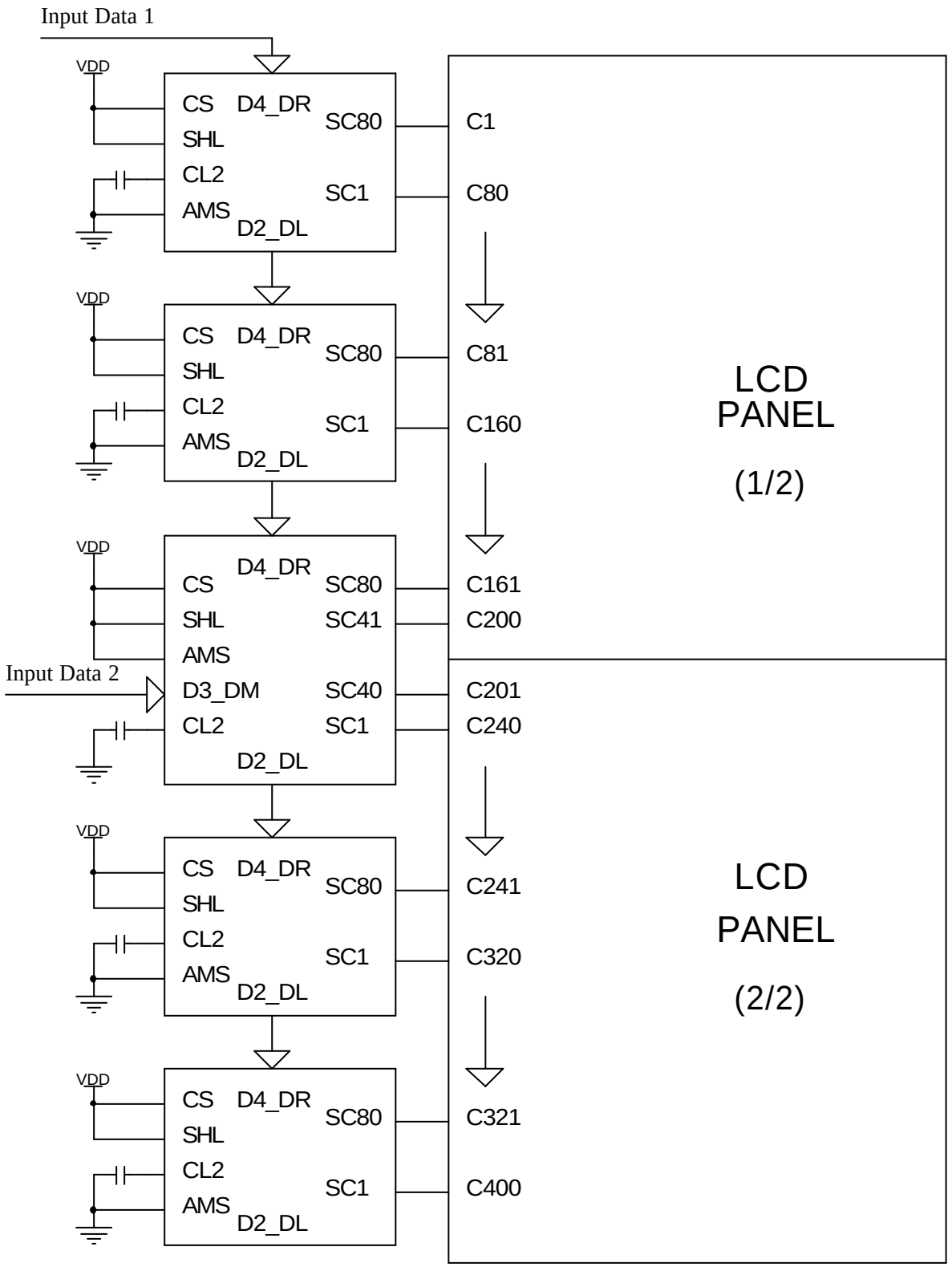
b) Upper View (SHL = H, AMS = L)



Single-type Interface Mode (80 Ch. Common Driver)



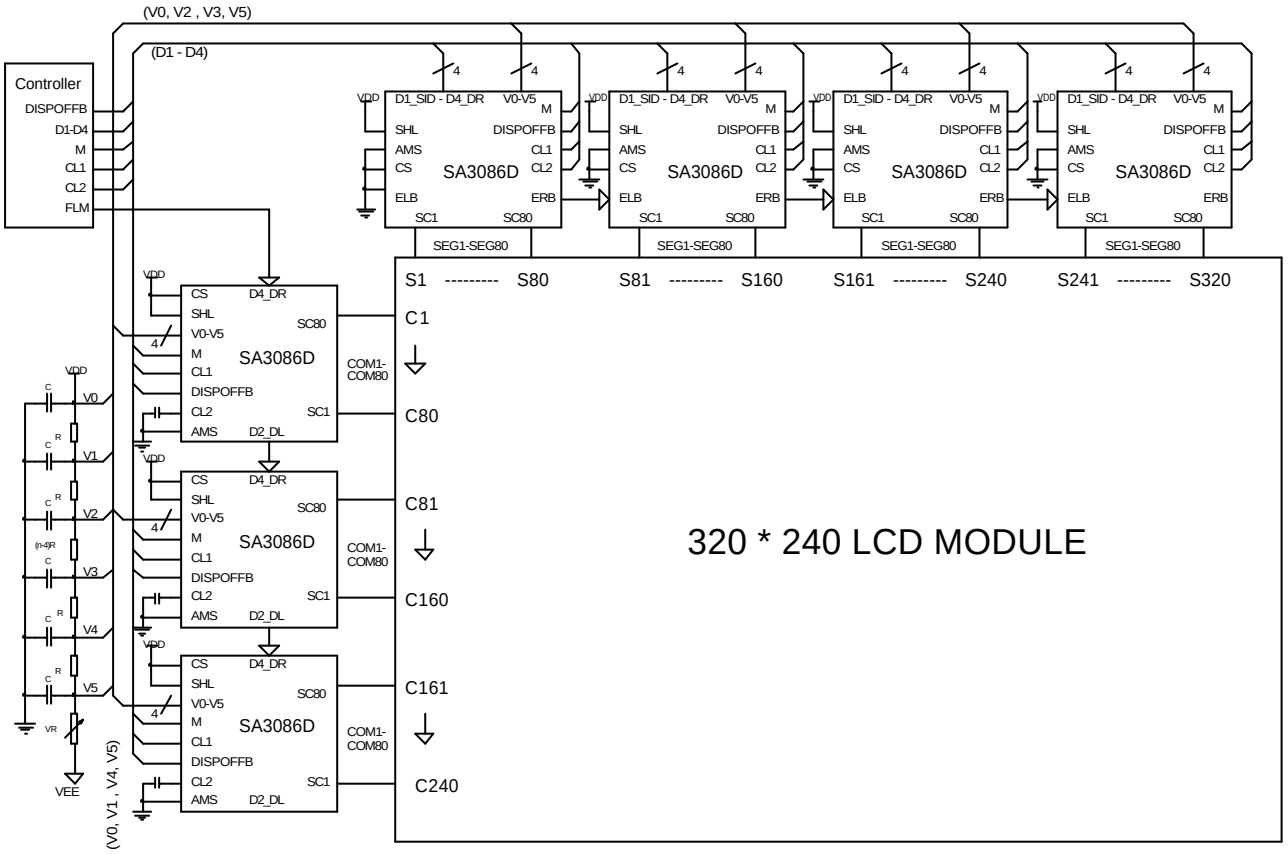
Dual-type Interface Mode (40 Ch. Common Driver)



Note: Using this application mode (dual-type common mode), the duty ratio can be reduced to half, in case, 1/200 duty can be used to drive the 400 common LCD panel.

Application Circuit Example (1)

Using SA3086D for 320 x 240



The 0.1uF capacitors add on the CL2 signal of common chip is reset internal circuit for standby mode.