SA3128

Technical Specification

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1. Description

The SA3128 is a 128-output segment/common driver IC suitable for driving small/medium scale dot matrix LCD panels. The SA3128 is good as a segment driver, a common driver or a common/segment driver, and it can create low power consumption, high-resolution LCD. The SA3128 have eight modes can selected to set common and segment numbers by selecting pin.

2. Features

Numbers of LCD drive outputs: 128

- Supply voltage for LCD drive (V_{OUT}): Max 30V
- Supply voltage for logic system (V_{DD}): +2.7 ~ +5.5V
- Low power consumption and low output impedance
- Display duty selectable by hardware configure.

DU3	DU2	DU1	DU0	COM Num.	SEG Num.
0	0	0	0	0	128
0	0	0	1	16	112
0	0	1	0	32	96
0	0	1	1	48	80
0	1	0	0	64	64
0	1	0	1	80	48
0	1	1	0	96	32
0	1	1	1	112	16
1	X	X	X	128	0

- Package: 154-pin COB.

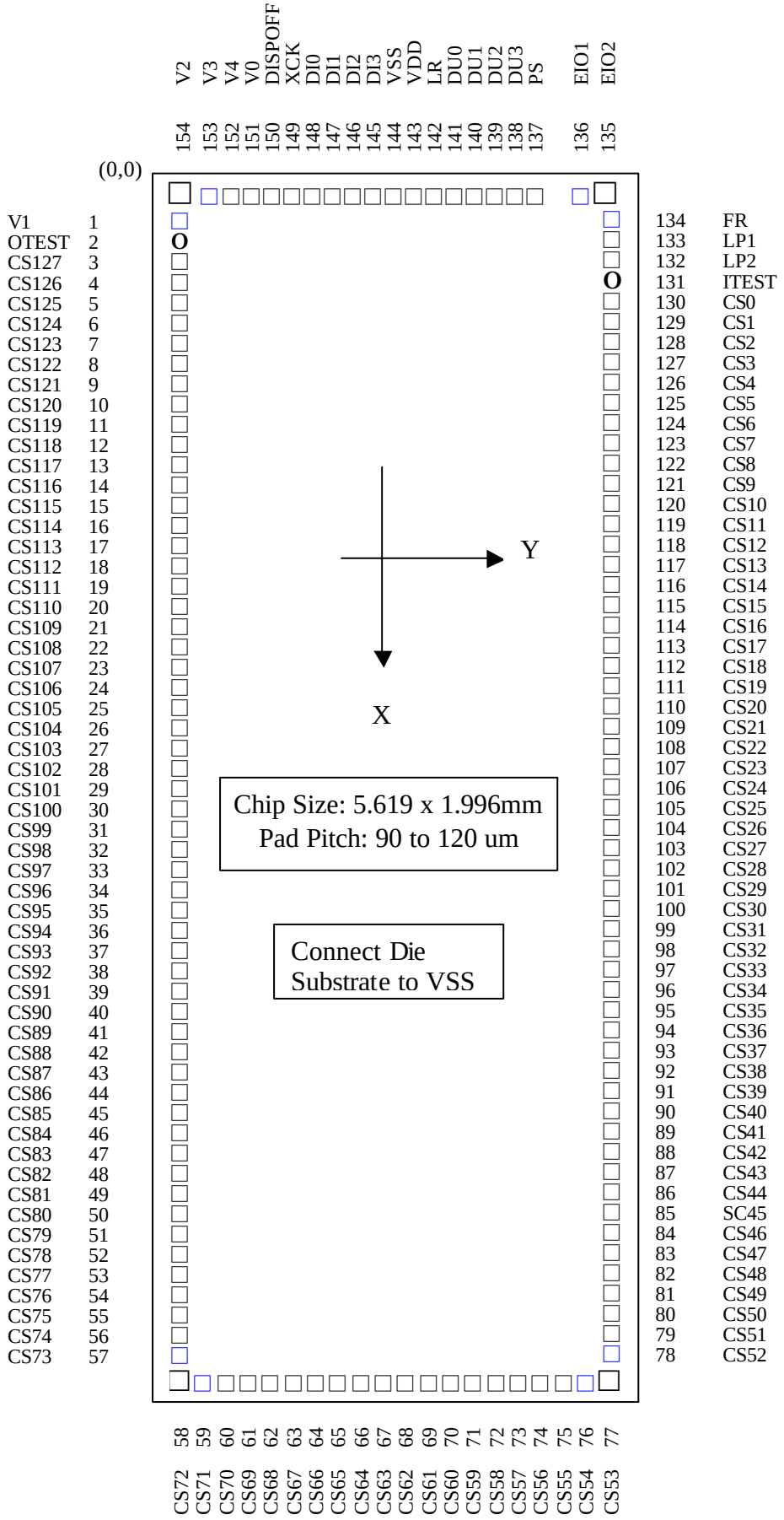
(Segment mode)

- Shift clock frequency
  - 20MHz (Max.): V_{DD} = +5.0 ± 0.5 V
  - 15MHz (Max.): V_{DD} = +3.0 to + 4.5 V
  - 12MHz (Max.): V_{DD} = +2.7 to + 3.0 V
- 4-bit parallel / serial input modes are selectable by PS pin.
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 16 32 48 64 80 96 112 128 bits of input data.
- Line latch circuits are reset when DISPOFF active.

(Common mode)

- Shift clock frequency: 4MHz (Max.)
- Available bi-directional shift register
  - In sequence and reverse order for common mode
  - Common and segment should be identical direction for mix mode
- Shift register circuits are reset when DISPOFF active

3. Pad Diagram



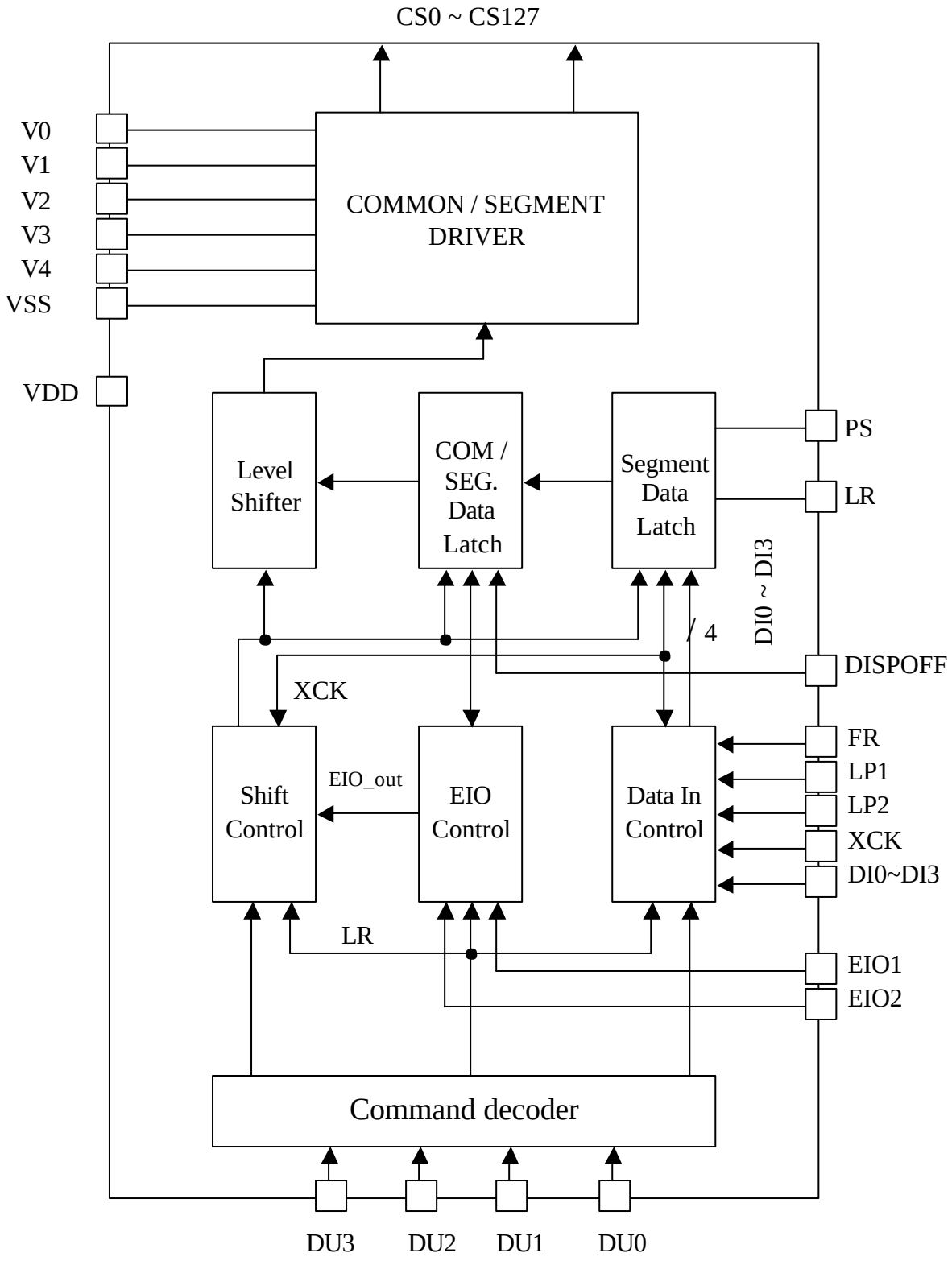
4. Pad Coordinates

No	Name	Coordinates	
		X	Y
1	V1	230.00	70.00
2	OTEST	350.00	70.00
3	CS127	450.00	70.00
4	CS126	550.00	70.00
5	CS125	644.90	70.00
6	CS124	754.90	70.00
7	CS123	844.90	70.00
8	CS122	934.90	70.00
9	CS121	1024.90	70.00
10	CS120	1114.90	70.00
11	CS119	1204.90	70.00
12	CS118	1294.90	70.00
13	CS117	1384.90	70.00
14	CS116	1474.90	70.00
15	CS115	1564.90	70.00
16	CS114	1654.90	70.00
17	CS113	1744.90	70.00
18	CS112	1834.90	70.00
19	CS111	1924.90	70.00
20	CS110	2014.90	70.00
21	CS109	2104.90	70.00
22	CS108	2194.90	70.00
23	CS107	2284.90	70.00
24	CS106	2374.90	70.00
25	CS105	2464.90	70.00
26	CS104	2554.90	70.00
27	CS103	2644.90	70.00
28	CS102	2734.90	70.00
29	CS101	2824.90	70.00
30	CS100	2914.90	70.00
31	CS99	3004.90	70.00
32	CS98	3094.90	70.00
33	CS97	3184.90	70.00
34	CS96	3274.90	70.00
35	CS95	3364.90	70.00
36	CS94	3454.90	70.00
37	CS93	3544.90	70.00
38	CS92	3634.90	70.00
39	CS91	3724.90	70.00
40	CS90	3814.90	70.00
41	CS89	3904.90	70.00
42	CS88	3994.90	70.00
43	CS87	4084.90	70.00
44	CS86	4174.90	70.00
45	CS85	4264.90	70.00
46	CS84	4354.90	70.00
47	CS83	4444.90	70.00
48	CS82	4534.90	70.00
49	CS81	4624.90	70.00
50	CS80	4714.90	70.00
51	CS79	4804.90	70.00
52	CS78	4894.90	70.00

No	Name	Coordinates	
		X	Y
53	CS77	4984.90	70.00
54	CS76	5098.05	70.00
55	CS75	5198.05	70.00
56	CS74	5298.05	70.00
57	CS73	5418.05	70.00
58	CS72	5538.05	80.00
59	CS71	5548.05	198.15
60	CS70	5548.05	292.15
61	CS69	5548.05	386.15
62	CS68	5548.05	480.15
63	CS67	5548.05	574.15
64	CS66	5548.05	668.15
65	CS65	5548.05	762.15
66	CS64	5548.05	856.15
67	CS63	5548.05	950.15
68	CS62	5548.05	1044.15
69	CS61	5548.05	1138.15
70	CS60	5548.05	1232.15
71	CS59	5548.05	1326.15
72	CS58	5548.05	1420.15
73	CS57	5548.05	1514.15
74	CS56	5548.05	1608.15
75	CS55	5548.05	1702.15
76	CS54	5548.05	1796.15
77	CS53	5538.05	1925.65
78	CS52	5418.05	1925.65
79	CS51	5298.05	1925.65
80	CS50	5198.05	1925.65
81	CS49	5098.05	1925.65
82	CS48	4984.90	1925.65
83	CS47	4894.90	1925.65
84	CS46	4804.90	1925.65
85	CS45	4714.90	1925.65
86	CS44	4624.90	1925.65
87	CS43	4534.90	1925.65
88	CS42	4444.90	1925.65
89	CS41	4354.90	1925.65
90	CS40	4264.90	1925.65
91	CS39	4174.90	1925.65
92	CS38	4084.90	1925.65
93	CS37	3994.90	1925.65
94	CS36	3904.90	1925.65
95	CS35	3814.90	1925.65
96	CS34	3724.90	1925.65
97	CS33	3634.90	1925.65
98	CS32	3544.90	1925.65
99	CS31	3454.90	1925.65
100	CS30	3364.90	1925.65
101	CS29	3274.90	1925.65
102	CS28	3184.90	1925.65
103	CS27	3094.90	1925.65
104	CS26	3004.90	1925.65

No	Name	Coordinates	
		X	Y
105	CS25	2914.90	1925.65
106	CS24	2824.90	1925.65
107	CS23	2734.90	1925.65
108	CS22	2644.90	1925.65
109	CS21	2554.90	1925.65
110	CS20	2464.90	1925.65
111	CS19	2374.90	1925.65
112	CS18	2284.90	1925.65
113	CS17	2194.90	1925.65
114	CS16	2104.90	1925.65
115	CS15	2014.90	1925.65
116	CS14	1924.90	1925.65
117	CS13	1834.90	1925.65
118	CS12	1744.90	1925.65
119	CS11	1654.90	1925.65
120	CS10	1564.90	1925.65
121	CS9	1474.90	1925.65
122	CS8	1384.90	1925.65
123	CS7	1294.90	1925.65
124	CS6	1204.90	1925.65
125	CS5	1114.90	1925.65
126	CS4	1024.90	1925.65
127	CS3	934.90	1925.65
128	CS2	844.90	1925.65
129	CS1	754.90	1925.65
130	CS0	664.90	1925.65
131	ITEST	550.00	1925.65
132	LP2	450.00	1925.65
133	LP1	350.00	1925.65
134	FR	230.00	1925.65
135	EIO2	80.00	1915.65
136	EIO1	70.00	1807.55
137	PS	70.00	1627.55
138	DU3	70.00	1537.55
139	DU2	70.00	1447.55
140	DU1	70.00	1357.55
141	DU0	70.00	1267.55
142	LR	70.00	1177.55
143	VDD	70.00	1087.55
144	VSS	70.00	997.55
145	DI3	70.00	907.55
146	DI2	70.00	817.55
147	DI1	70.00	727.55
148	DI0	70.00	637.55
149	XCK	70.00	547.55
150	DISPOFF	70.00	457.55
151	V0	70.00	367.55
152	V4	70.00	277.55
153	V3	70.00	187.55
154	V2	80.00	80.00

5. Block Diagram



6. Pin Description

Symbol	I/O	Description
CS0~CS127	O	LCD drive output
V0~V4	P	Power supply for LCD drive
VDD	P	Power supply for logic system (+2.7 to +5.5V)
EIO2, EIO1	I/O	Input/output for chip selection at segment/common mode and FLM input output function at common/segment mix mode or common mode Shift direction is accord LR setting included segment and common direction
DI0~DI3	I	Display data input at segment mode
DU0~DU3	I	Selected setting of duties for segment or common
XCK	I	Clock input for taking display data at segment mode
DISPOFF	I	Control input for output of ground level
LP1	I	Latch pulse input for display data at segment mode
LP2	I	Shift clock input for shift register at common mode
FR	I	AC-converting signal input for LCD drive waveform
VSS	P	Ground (0V)
PS	I	Serial or 4 bits mode selected pin
LR	I	Selected shift direction of segment and common are decided to EIO input or output

7. Pin Function Description

7.1 Pin Functions

(Segment mode)

Symbol	Function
VDD	Logic system power supply pin, connected to +2.7 to +5.5V
VSS	Ground pin, connected to 0V
V0, V1, V2, V3, V4	Supply the bias voltages input to drive the LCD. Ensure that voltages are set such that V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ Vss
DI0 ~ DI3	Input pins for display data In 4-bit parallel input mode, connect data to the 4 pins, DI0 ~ DI3. In serial input mode, connect data to the DI0 pin, and DI1-DI3 must be connected to Vss. Refer to "Relationship between the display data and LCD drive output Pins" in Functional Operations
LP1	Latch pulse input pin for display data Data is latched at the falling edge of the clock pulse.
XCK	Clock input for taking display data at the segment mode.
DISPOFF	The switch for turn on or turn off the LCD display The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. When set to DISPOFF is 'L', the LCD drive output pins (CS0-CS127) are set to level Vss. When set to 'L', the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of DISPOFF. When the DISPOFF function is canceled, the driver outputs non-select level (V2 or V3), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if DISPOFF removal time does not correspond to what shown in AC characteristics, it cannot output the reading data correctly. Table of truth-values is shown in 'Truth Table' in Functional Operations.
FR	AC signal input pin for LCD drive waveform The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. Normally it inputs a frame inversion signal. The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. Table of truth-values is shown in 'Truth table' in Functional Operations
EIO1, EIO2	Input / output pins for chip selection. When LR is set '0'. EIO1 is set for output, and EIO2 is set for input (connect to Vss) When LR is set '1'. EIO1 is set for input (connect to Vss), and EIO2 is set for output. During output, set to 'H' while LP and XCK is 'H' and after 127 bits of data have been read, set to 'L' for one cycle (from falling edge to falling edge of XCK), after which it returns to 'H'. During input, the chip is selected while EIO is set to 'L' after the LP signal is input. The chip is non-selected after 128 bits of data have been read.
CS0 ~ CS127	LCD drive output pins Corresponding directly to each bit of the data latch, one level (V0, V2, V3, Vss) is selected are output. Table of truth values are shown in 'Truth Table' in Functional Operations.

(Common mode)

Symbol	Function
VDD	Logic system power supply pin, connected to +2.7 to +5.5V
VSS	Ground pin, connected to 0V
V0, V1, V2, V3, V4	Supply the bias voltages input to drive the LCD. Ensure that voltages are set such that V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ Vss
DI0 ~ DI3	Not used. Connect DI0-DI3 to Vss, not floating.
LP2	Shift clock pulse input pin for bi-directional shift register * Data is shifted at the falling edge of the clock pulse. When use gray scale mode, and then must use the pin. When use monochrome mode, then the pin should be shorted to LP1.
XCK	Not used Not let it floating, connect to Vss.
DISPOFF	The switch for turn on or turn off the LCD display The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. When set to DISPOFF is "L", the LCD drive output pins (CS0-CS127) are set to level Vss. When set to 'L', the contents of the shift register are reset to not reading data. When the DISPOFF function is canceled, the driver outputs non-select level (V1 or V4), and the shift data is read at the next falling edge of the LP. At that time, if DISPOFF removal time does not correspond to what shown in AC characteristics, it cannot output the reading data correctly. Table of truth-values is shown in 'Truth Table' in Functional Operations.
FR	AC signal input pin for LCD drive waveform The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. Normally it inputs a frame inversion signal. The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. Table of truth-values is shown in 'Truth table' in Functional Operations
CS0 ~ CS127	LCD drive output pins Corresponding directly to each bit of the data latch, one level (V0, V1, V4, Vss) is selected is output. Table of truth values is shown in 'Truth Table' in Functional Operations.
EIO1, EIO2	Shift data Input / output pins for shift register EIO1 is output when LR is at Vss level 'L', EIO1 I input pin when LR is at V_{DD} level 'H' When LR register = '1', EIO1 is used as input pin, it will be connect to FLM. When LR register = '0', EIO1 is used as output pin, it will be connect to next chip. EIO2 is input pin when LR is at Vss level 'L', EIO1 is output pin when LR is at V_{DD} level 'H' When LR register = '1', EIO2 is used as output pin, it will be connect to next chip. When LR register = '0', EIO2 is used as input pin, it will be connect to FLM Refer to 'Relationship between the display data and LCD drive output pins' in Function Operations.

(Common / Segment mix mode)

Symbol	Function
VDD	Logic system power supply pin, connected to +2.7 to +5.5V
VSS	Ground pin, connected to 0V
V0, V1, V2, V3, V4	Supply the bias voltages input to drive the LCD. Ensure that voltages are set such that V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ Vss
DI0~ DI3	Input pins for display data In 4-bit parallel input mode, connect data to the 4 pins, DI0 ~ DI3. In serial input mode, connect data to the DI0 pin, and DI1-DI3 must be connected to Vss. Refer to Relationship between the display data and LCD drive output pins in Functional Operation
XCK	Clock input for taking display data Data is read at the falling edge of clock pulse.
LP1	Latch pulse input pin for display data Data is latched at the falling edge of the clock pulse.
LP2	Shift clock pulse input pin for bi-directional shift register Data is shifted at the falling edge of the clock pulse. When use gray scale mode, and then must use the pin. When use monochrome mode, then the pin should be shorted to LP1.
FR	AC signal input pin for LCD drive waveform The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal, and inputs at frame inversion signal normally. Table of truth-values is shown in 'Truth table' in Functional Operations
DISPOFF	The switch for turn on or turn off the LCD display The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. When set to DISPOFF is 'L', the LCD drive output pins (CS0-CS127) are set to level Vss. When set to 'L', the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of DISPOFF. When the DISPOFF function is canceled, the driver outputs non-select level (V2 or V3), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if DISPOFF removal time does not correspond to what shown in AC characteristics, it cannot output the reading data correctly. Table of truth-values is shown in 'Truth Table' in Functional Operations.
EIO1, EIO2	Input / output pins for chip selection. When LR register is set '0'. EIO1 is set for output, and EIO2 is ser for input EIO1: segment chip enable output, as default segment enabled internally and be non-selected after 16, 32, 48, 64, or 80, 96, 112 bits of data have been read. Depend on select mode. EIO2: common shift data input, no shift data output When LR register is set '1'. EIO1 is set for input, and EIO2 is set for output. EIO1: common shift data input, or shift data output EIO2: segment chip enable output, as default segment enabled internally and be non-selected after 16, 32, 48, 64, or 80, 96, 112 bits of data have been read. Depend on select mode. During output, set to 'H' while LP and XCK is 'H' and after 128 bits of data have been read, set to 'L' for one cycle (from falling edge to falling edge of XCK), after which it returns to 'H'. During input, the chip is selected while EIO is set to 'L' after the LP signal is input. The chip is non-selected after 128 bits of data have been read.
CS0 ~ CS127	LCD drive output pins Corresponding to each bit of the data latch, one level (V0, V2, V3, Vss) is selected are output. Table of truth values is shown in 'Truth Table' in Functional Operations.

7.2 Functional Operations

7.2.1 Truth Table

(Segment Mode)

FR	Latch Data	DISPOFF	LCD Drive Output Voltage Level (CS0-CS127)
L	L	H	V3
L	H	H	Vss
H	L	H	V2
H	H	H	V0
X	X	L	Vss

(Common Mode)

FR	Latch Data	DISPOFF	LCD Drive Output Voltage Level (CS0-CS127)
L	L	H	V4
L	H	H	V0
H	L	H	V1
H	H	H	Vss
X	X	L	Vss

Notes:

X: Don't care should be fixed to 'H' or 'L', avoiding floating.

There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage that is assigned by specification for each power pin.

7.2.2 Relationship Between the Display Data and LCD drive Output Pins

(Segment mode)

(A) 4-bit Parallel Input Mode

LR	EIO1	EIO2	Data Input	Number of clocks						
				32 clock	31 clock	30 clock	…	3 clock	2 clock	1 clock
L	Output	Input	DI0	CS0	CS4	CS8	…	CS116	CS120	CS124
			DI1	CS1	CS5	CS9	…	CS117	CS121	CS125
			DI2	CS2	CS6	CS10	…	CS118	CS122	CS126
			DI3	CS3	CS7	CS11	…	CS119	CS123	CS127
H	Input	Output	DI0	CS127	CS123	CS119	…	CS11	CS7	CS3
			DI1	CS126	CS122	CS118	…	CS10	CS6	CS2
			DI2	CS125	CS121	CS117	…	CS9	CS5	CS1
			DI3	CS124	CS120	CS116	…	CS8	CS4	CS0

(B) Serial Input Mode

LR	EIO1	EIO2	Data Input	Number of clocks						
				128 clock	127 clock	126 clock	…	3 clock	2 clock	1 clock
L	Output	Input	DI0	CS0	CS1	CS2	…	CS125	CS126	CS127
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X
H	Input	Output	DI0	CS127	CS126	CS125	…	CS2	CS1	CS0
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X

(Common mode)

LR	Data Transfer Direction
L	CS127→CS0
H	CS0→CS127

Mix Mode (Segment / Common mode)

When (DU3, DU2, DU1, DU0)=(0, 0, 1, 0)→ Select the 32 COM / 96 Segment mode

Then Segment Side of mix mode

(A) 4-bit Parallel Input Mode

LR	EIO1	EIO2	Data Input	Number of clocks						
				24 clock	23 clock	22 clock	…	3 clock	2 clock	1 clock
L	Seg_end Output	Com_FLM Input	DI0	CS0	CS4	CS8	…	CS84	CS88	CS92
			DI1	CS1	CS5	CS9	…	CS85	CS89	CS93
			DI2	CS2	CS6	CS10	…	CS86	CS90	CS94
			DI3	CS3	CS7	CS11	…	CS87	CS91	CS95
H	Com_FLM Input	Seg_end Output	DI0	CS127	CS123	CS119	…	CS43	CS39	CS35
			DI1	CS126	CS122	CS118	…	CS42	CS38	CS34
			DI2	CS125	CS121	CS117	…	CS41	CS37	CS33
			DI3	CS124	CS120	CS116	…	CS40	CS36	CS32

(B) Serial Input Mode

LR	EIO1	EIO2	Data Input	Number of clocks						
				96 clock	95 clock	94 clock	…	3 clock	2 clock	1 clock
L	Seg_end Output	Com_FLM Input	DI0	CS0	CS1	CS2	…	CS93	CS94	CS95
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X
H	Com_FLM Input	Seg_end Output	DI0	CS127	CS126	CS125	…	CS34	CS33	CS32
			DI1	X	X	X	X	X	X	X
			DI2	X	X	X	X	X	X	X
			DI3	X	X	X	X	X	X	X

Common side of mix mode

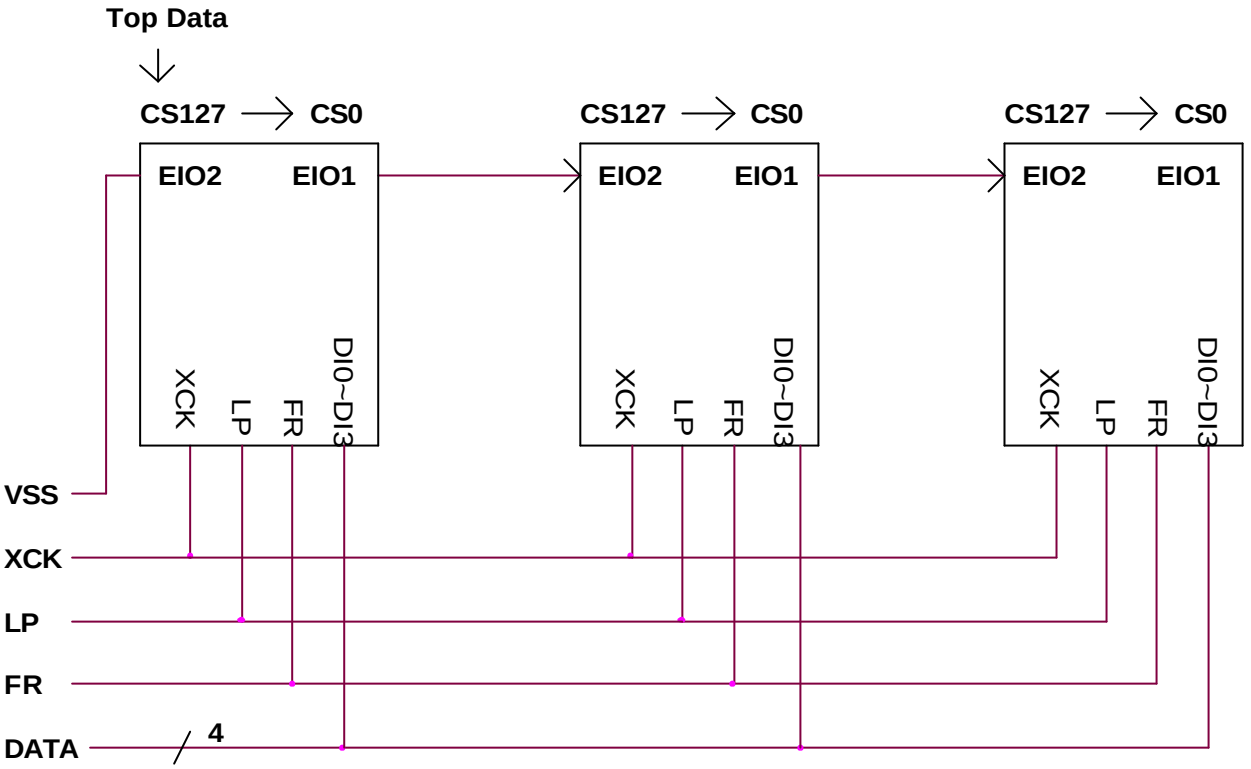
LR	Data Transfer Direction
L	CS127→CS96
H	CS0→CS31

Notes:

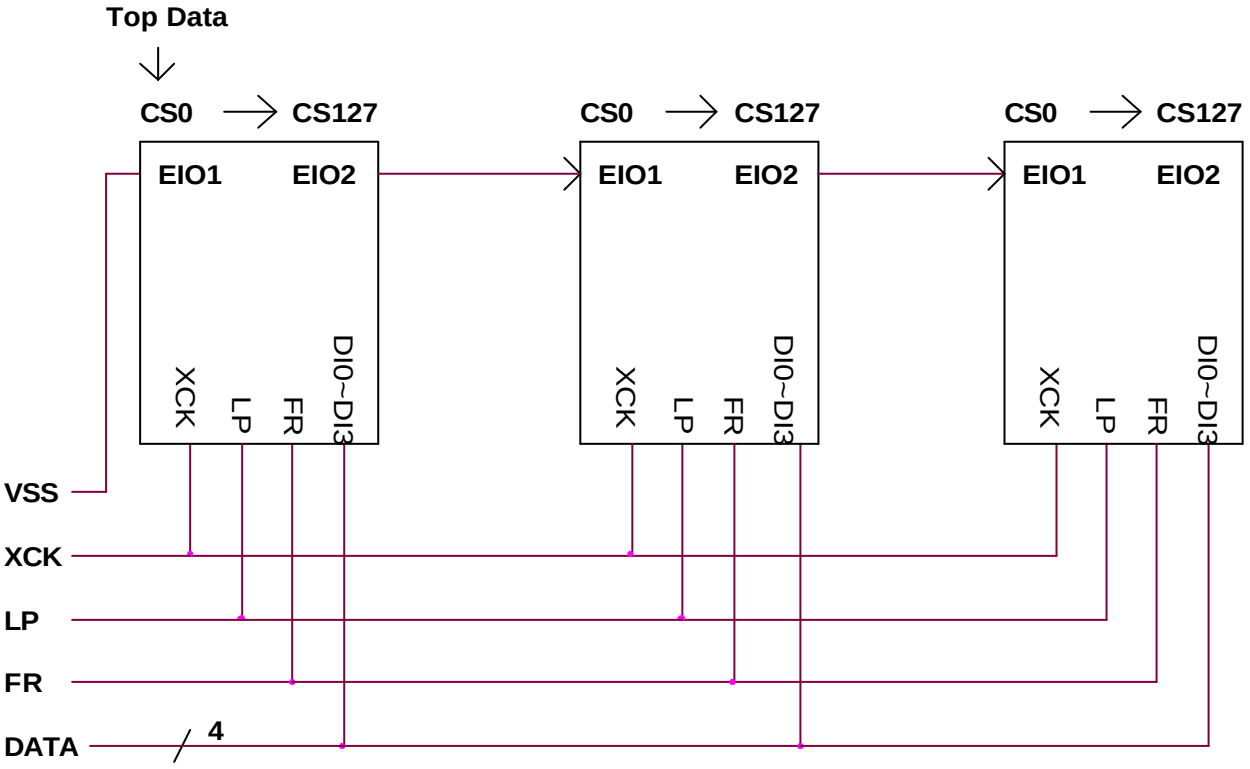
X: Don’t care should be fixed to ‘H’ or ‘L’, avoiding floating.

7.2.3 Connection examples of plural segment drivers in 4-bits interface

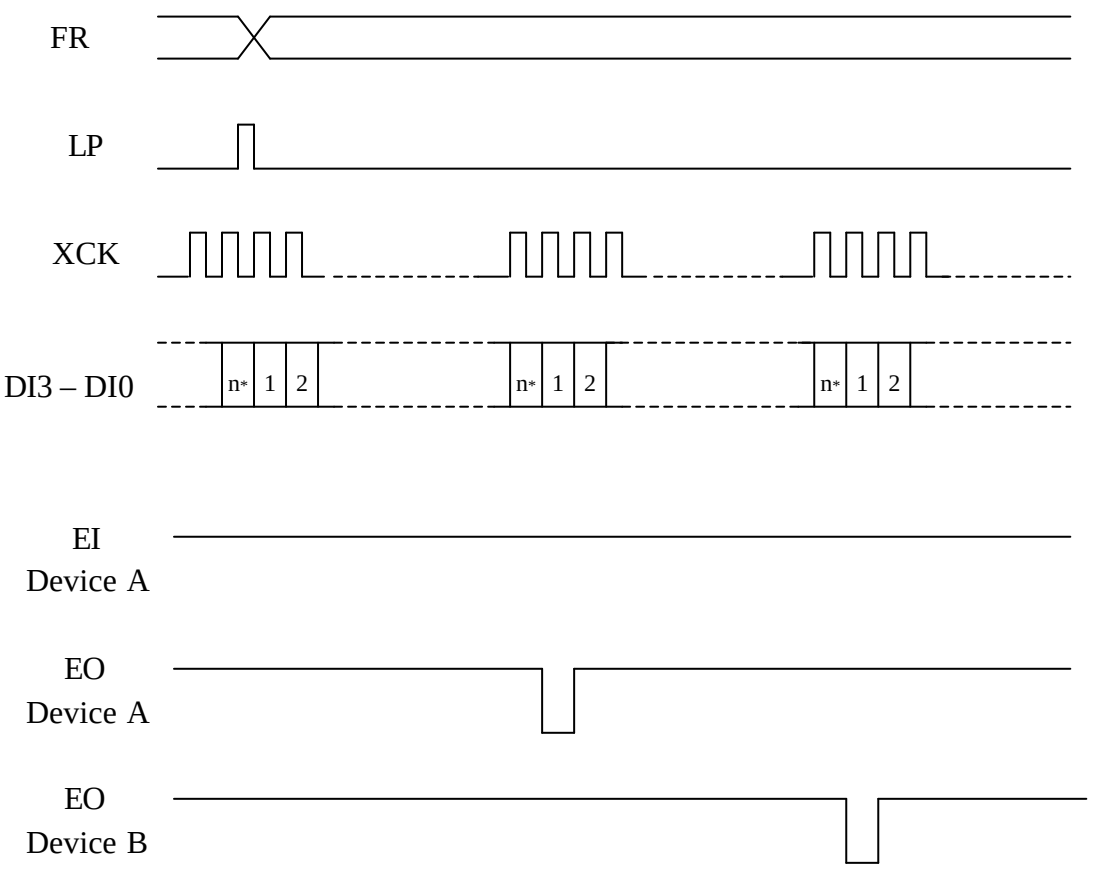
(a) When the LR pin set 'L' level



(b) When the LR pin set 'H' level



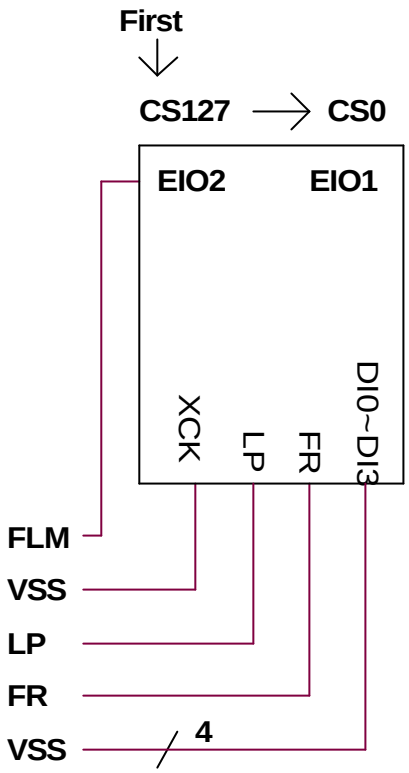
7.2.4 Timing chart of 4-device cascade connection of segment drivers



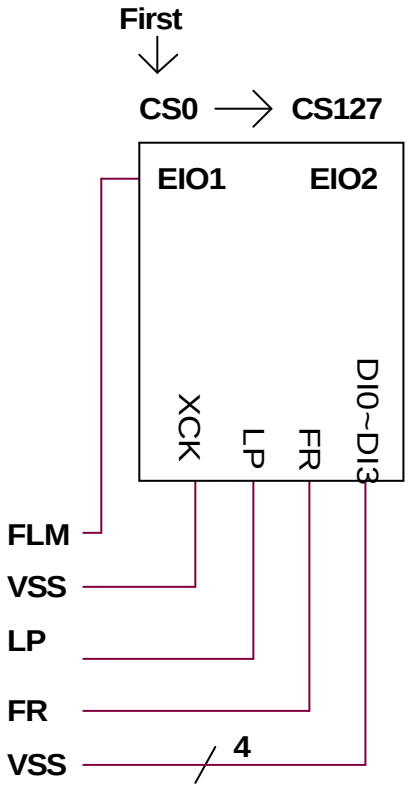
*n = 32 in 4bit parallel input mode
*n = 128 in serial input mode

7.2.5 Connection examples for signal common drivers

(c) LR pin set ‘L’ level



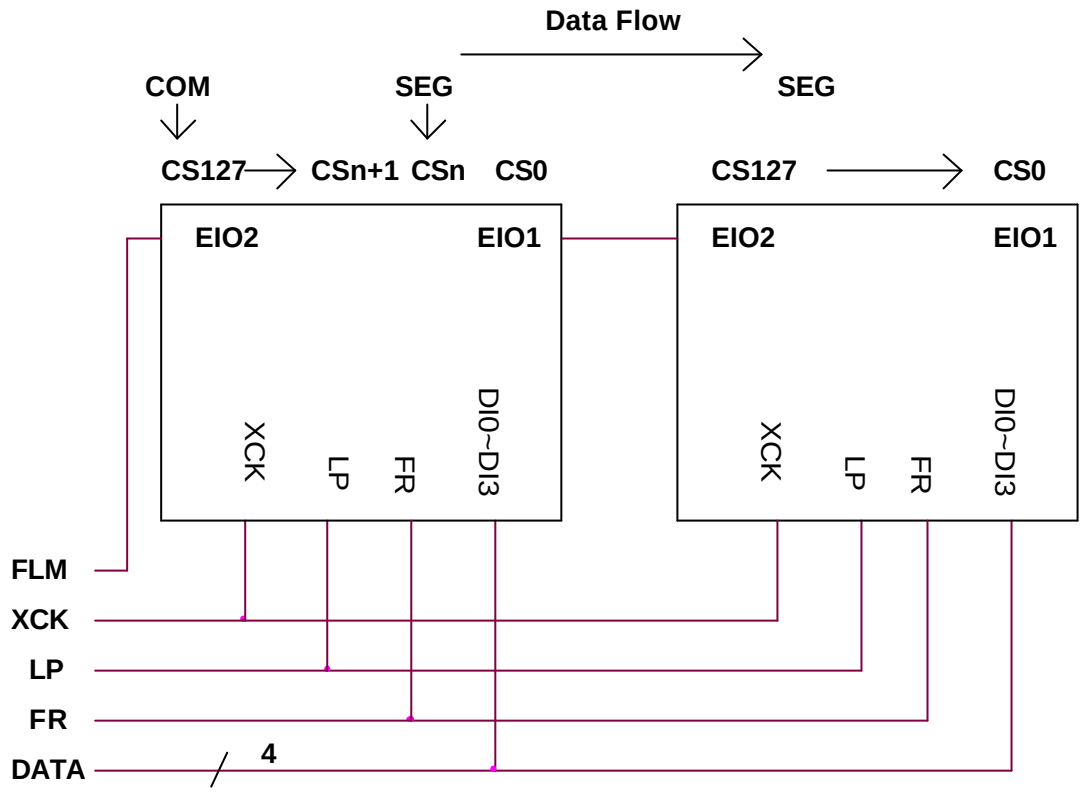
(d) LR pin set ‘H’ level



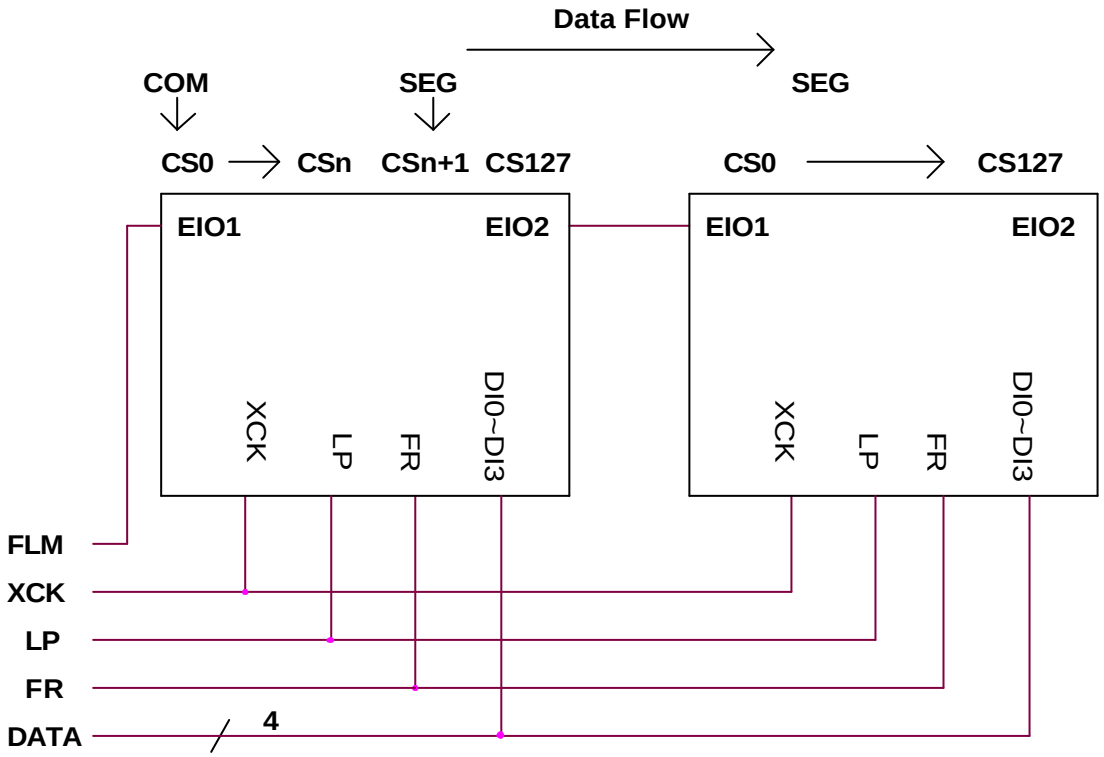
7.2.6 Connection examples for plural common/segment (mix mode) drivers

The mix mode is 1/16, 1/32, 1/48, 1/64, 1/80, 1/96, 1/112, 1/128 duty mode

(e) When the LR register set 'L' level



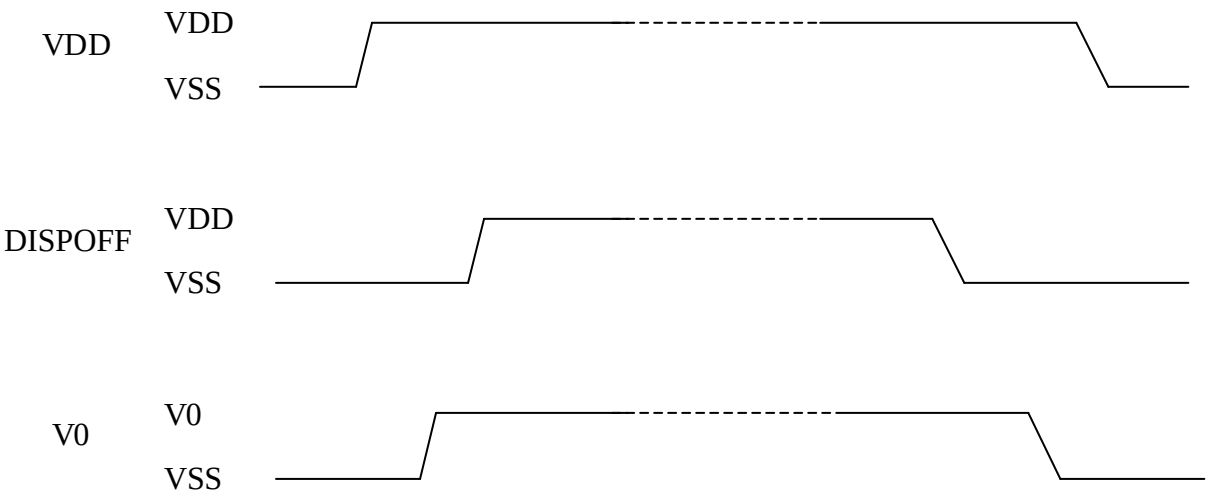
(f) When the LR register set 'H' level



8. Precautions

Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,
When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power
And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on DISPOFF function. After that, cancel the DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V0 on DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.
When connecting the power supply, follow the recommended sequence shown here



9. Hardware Circuit Description

The LCD Data Bus Interface

There are two kinds of interfaces for LCD data bus. One is 4-bit parallel data interface and the other is the serial interface. These two kinds of interfaces are selected by setting the Ps pin, and see detail in the Table 1. DI1~DI3 on data bus must be fixed to ground when PS bit is selected.

PS	Data Bus Mode
1	Parallel Interface (DI3~DI0)
0	Serial Interface (DI0)

Table 1

10. Absolute Maximum Ratings

Parameter	Symbol	Applicable Pin	Rating	Unit	Note
Supply voltage (1)	V_{DD}	V_{DD}	2.7 ~ 5.5	V	1,2
Supply voltage (2)	V1	V1	V_{DD}+10 ~ V_{DD}+0.3	V	
	V2	V2	V_{DD}+10 ~ V_{DD}+0.3	V	
	V3	V3	-0.3 ~ Vss +10	V	
	V4	V4	-0.3 ~ Vss +10	V	
Input voltage	VI	DI3-DI0, XCK, FR, EIO1, EIO2, DISPOFF	-0.3 to V_{DD} +0.3	V	
Storage temperature	T_{STG}		-45 to +125	°C	

Notes:

1. Ta = +25°C
2. The maximum applicable voltage on any pin with respect to Vss (0V)

11 Recommended Operating Conditions

Parameter	Symbol	Applicable Pins	Min.	Typ.	Max.	Unit	Note
Supply voltage (1)	V_{DD}	V_{DD}	+2.7		+5.5	V	1,2
Supply voltage (2)	V0	V0	+15		+30.0	V	
Operation temperature	T_{OPR}		-20		+85	°C	

Notes:

1. The applicable voltage on any pin with respect to Vss (0V).
2. Ensure that voltages are set such that V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ Vss

12. Electrical Characteristics

12.1 DC Characteristics

(Segment Mode)

(Vss = 0V, V_{DD} = +2.7 to +5.5V, V0 = 15 to 30.0V, T_{OPR} = -20 to 85°C)

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit	Note
Input 'Low' voltage	V_{IL}		DI3-DI0, XCK, FR, EIO1, EIO2, DISPOFF			$0.2V_{DD}$	V	
Input 'High' voltage	V_{IH}			$0.8V_{DD}$			V	
Output 'Low' voltage	V_{OL}	I_{OL} = +0.4mA	EIO1, EIO2			+0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = Vss	DI3-DI0, XCK, LP, FR, EIO, EIO2, DISPOFF			-10	µA	
	I_{LIH}	V_I = V_{DD}				+10	µA	
Output resistance	R_{ON}	$\|\Delta V_{ON}\|$ = 0.5V, V0 = 30V	CS0 – CS127		1.0	1.5	kΩ	
Standby current	I_{STS}		Vss			3.0	µA	1
Output current	I1 to I4		V1, V2, V3, V4			300	µA	

Notes: V_{DD} = +3.0V, V0 = 30.0V, V_I = Vss

(Common Mode)

(Vss = 0V, V_{DD} = +2.7 to +5.5V, V0 = 15 to 30.0V, T_{OPR} = -20 to 85°C)

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit	Note
Input 'Low' voltage	V_{IL}		DI3-DI0, XCK, FR, EIO1, EIO2, DISPOFF			$0.2V_{DD}$	V	
Input 'High' voltage	V_{IH}			$0.8V_{DD}$			V	
Output 'Low' voltage	V_{OL}	I_{OL} = +0.4mA	EIO1, EIO2			+0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = Vss	DI3-DI0, XCK, FR, P/S, EIO, EIO2, DISPOFF			-10	µA	
	I_{LIH}	V_I = V_{DD}	DI3-DI0, FR, DISPOFF			+10	µA	
Input pull-down current	I_{PO}	V_I = V_{DD}	XCK, EIO1, EIO2			100	µA	
Output resistance	R_{ON}	$\|\Delta V_{ON}\|$ = 0.5V, V0 = 30V	CS0-CS127		1.0	1.5	kΩ	
Standby current	I_{SPO}		Vss			3.0	µA	1
Supply current (1)	I_{DD}		V_{DD}			80	µA	2
Supply current (2)	I0		V0			130	µA	2

Notes:

1. V_{DD} = +3.3V, V0 = 30.0V, V_I = Vss
2. V_{DD} = +3.3V, V0 = 30.0V, f_{LP} = 19.2kHz, f_{FR} = 80Hz, 1/128 duty operation, no-load.

12.2 AC Characteristics

(Segment Mode 1)

(Vss = 0V, V_{DD} = +2.7 to +3.0V, V0 = 15 to 30.0V, T_{OPR} = -20 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Shift clock period	t_{WCK}	t_R, $t_F \le 11$ns	125			ns	1
Shift clock 'H' pulse width	t_{WCKH}		51			ns	
Shift clock 'L' pulse width	t_{WCKL}		51			ns	
Data setup time	t_{DS}		30			ns	
Data hold time	t_{DH}		40			ns	
Latch pulse 'H' pulse width	t_{WLPH}		51			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		51			ns	
Latch pulse fall to shift clock fall time	t_{LH}		51			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	ts		36			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF 'L' pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15pF			78	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15pF			1.2	µs	

Notes:
1. Takes the cascade connection into consideration
2. (t_{WCK} – t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2)

(Vss = 0V, V_{DD} = +5.0±0.5V, V0 = 15 to 30.0V, T_{OPR} = -20 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Shift clock period	t_{WCK}	t_R, $t_F \leq$ 10ns	66			ns	1
Shift clock 'H' pulse width	t_{WCKH}		23			ns	
Shift clock 'L' pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse 'H' pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	ts		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF 'L' pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15pF			1.2	µs	

Notes:
1. Takes the cascade connection into consideration
2. (t_{WCK}-t_{WCKH}-t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3)

(Vss = 0V, V_{DD} = +3.0 to +4.5V, V0 = 15 to 30.0V, T_{OPR} = -20 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Shift clock period	t_{WCK}	t_R, $t_F \leq$ 10ns	82			ns	1
Shift clock 'H' pulse width	t_{WCKH}		28			ns	
Shift clock 'L' pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse 'H' pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	ts		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF 'L' pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15pF			1.2	µs	

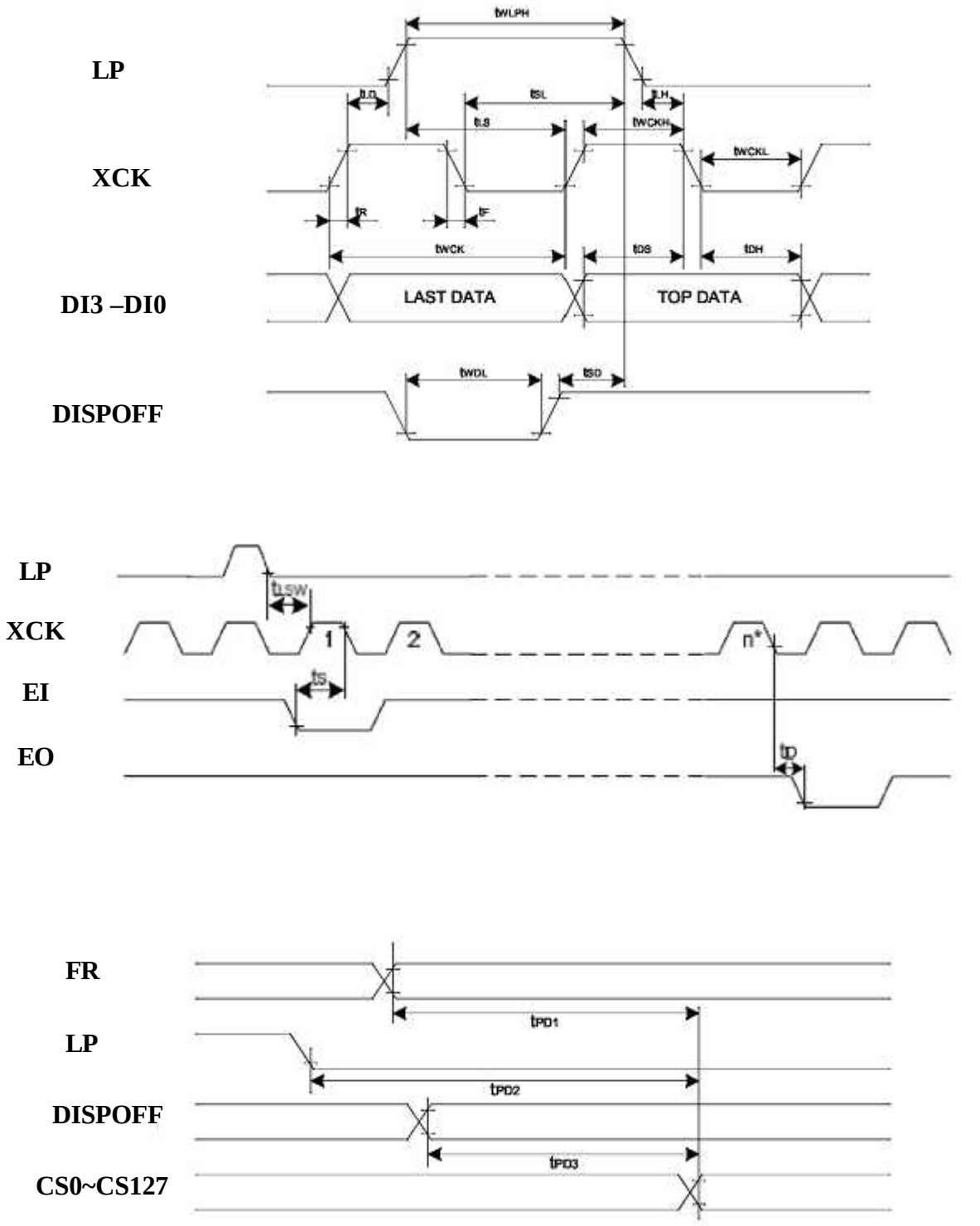
Notes:
1. Takes the cascade connection into consideration
2. (t_{WCK}-t_{WCKH}-t_{WCKL})/2 is maximum in the case of high speed operation.

(Common Mode)

(Vss = 0V, V_{DD} = +2.7 to +5.5V, V0 = 15 to 30.0V, T_{OPR} = -20 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period	t_{WLP}	t_R, $t_F \leq$ 20ns	250			ns
Shift clock 'H' pulse width	t_{WLPH}	V_{DD} = 5±0.5V	15			ns
		V_{DD} = 2.7 ~ 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF 'L' pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	CL = 10pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 10pF			1.2	µs
Output delay time (3)	t_{PD3}	CL = 10pF			1.2	µs

12.3 Timing Chart of Segment Mode

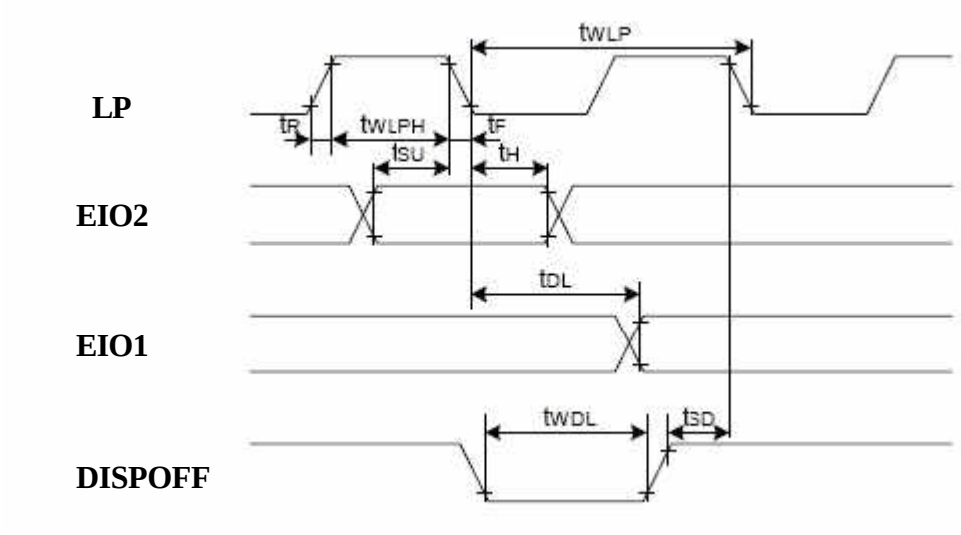


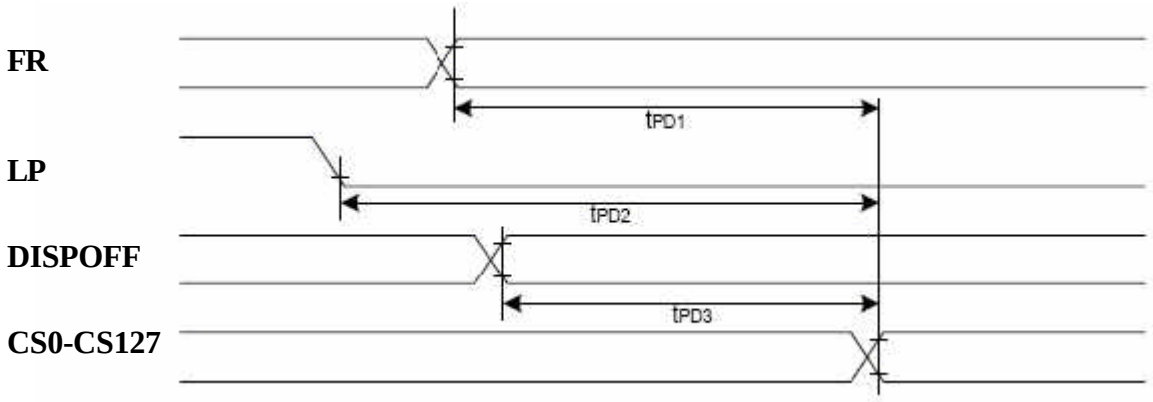
Timing Characteristics (3)

(Common Mode)

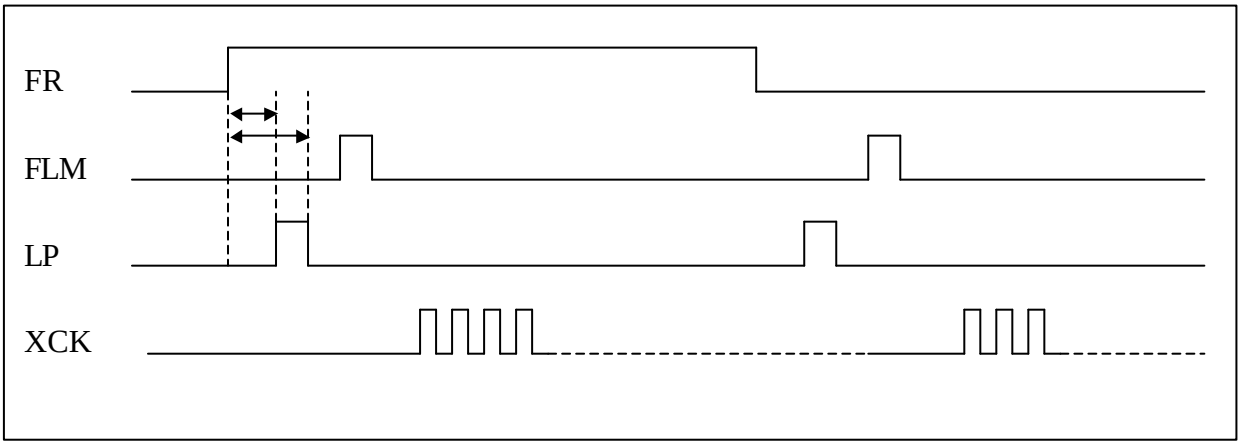
(Vss = 0V, VDD = +2.7 to 5.5V, V0 = 15 to 30.0V, TOPR = -20 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period	t_{WLP}	t_R, $t_F \leq 20ns$	250			ns
Shift clock 'H' pulse width	t_{WLPH}	VDD = 5±0.5V	15			ns
		VDD = 2.7 ~ 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF 'L' pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	CL = 10pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 10pF			1.2	µs
Output delay time (3)	t_{PD3}	CL = 10pF			1.2	µs





12.5 Application Timing Block:



* FR and LP falling edge must > 10ns

13. Application Circuit

When use one SA3128 in mix mode (96*32)