Alphanumeric Liquid crystal display (LCD) controller and driver

SA8016

Technical Specification

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Basic function

- Alphanumeric LCD controller driver
- Interface with 4/8-bit and serial interface microprocessors
- Extended control instruction system controller, display, data input or output
- Alphanumeric characters in one or two lines
- 16 common and 80 segment output

Features

- Character type for 5 x 8 dot matrix LCD controller and driver
- 19840 bit Character Generator ROM
  - 496 characters font 5x8 dot
- 512 bit Character Generate RAM
  - 64 x 8 bit for character fonts
- 80 characters Display RAM
- Lower power operation support: 2.7 to 3.3V
- Range of LCD driver power: 3.0 to 5.0V
- Support high speed serial interface
- Correspond to high speed MPU bus interface, easy with 4 bit and 8 bit interface
- Programmed number of common:
  - 1/8 for one line of 5x8 dots with cursor
  - 1/16 for two lines of 5x8 dots with cursor
- Built in power on reset circuit
- Built in oscillator circuit with external resistor
- Lower power consumption

Introduction

The SA8016 is a matrix liquid display (LCD) controller for the alphanumeric display. It has 16 common drivers (COM) and 80 segment drivers (SEG). This allows to displays one or two lines of characters 5x8 format.

The display character codes are written into the 80-byte Display Data RAM (DDRAM). The character patterns are stored in the 19840-bit Character Generator ROM (CGROM) or 64x8 bit Character Generator RAM (CGRAM). The CGROM consists of two banks with capacity 19840 bit each, and contains up of two pages 5x8 characters. In the CGRAM the user can write up to eight 5x8 characters.

SA8016 can interface with many types of 4/8/16 bit MPU. The controller has a wide instruction set and flexible functions.

Block Diagram

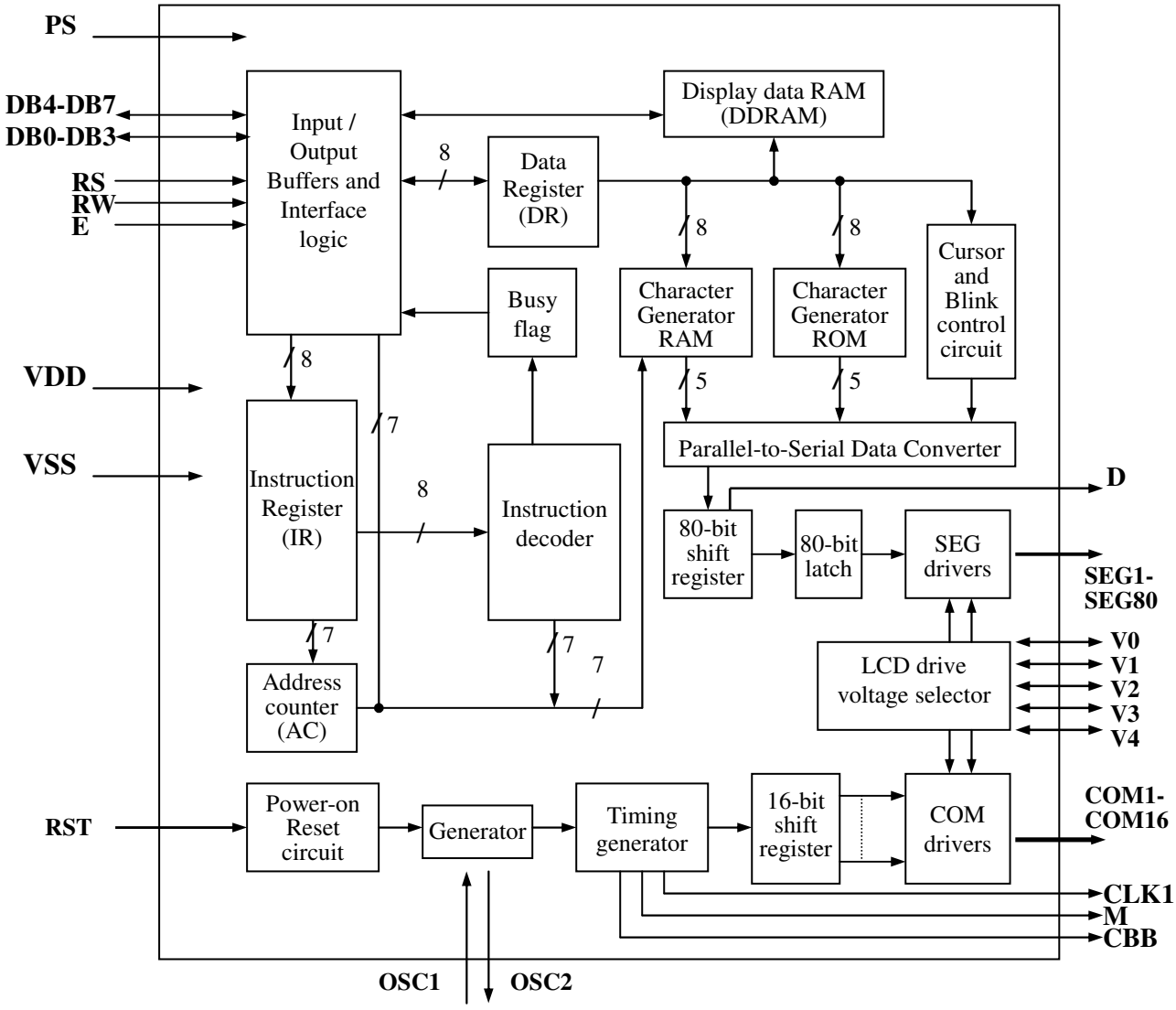
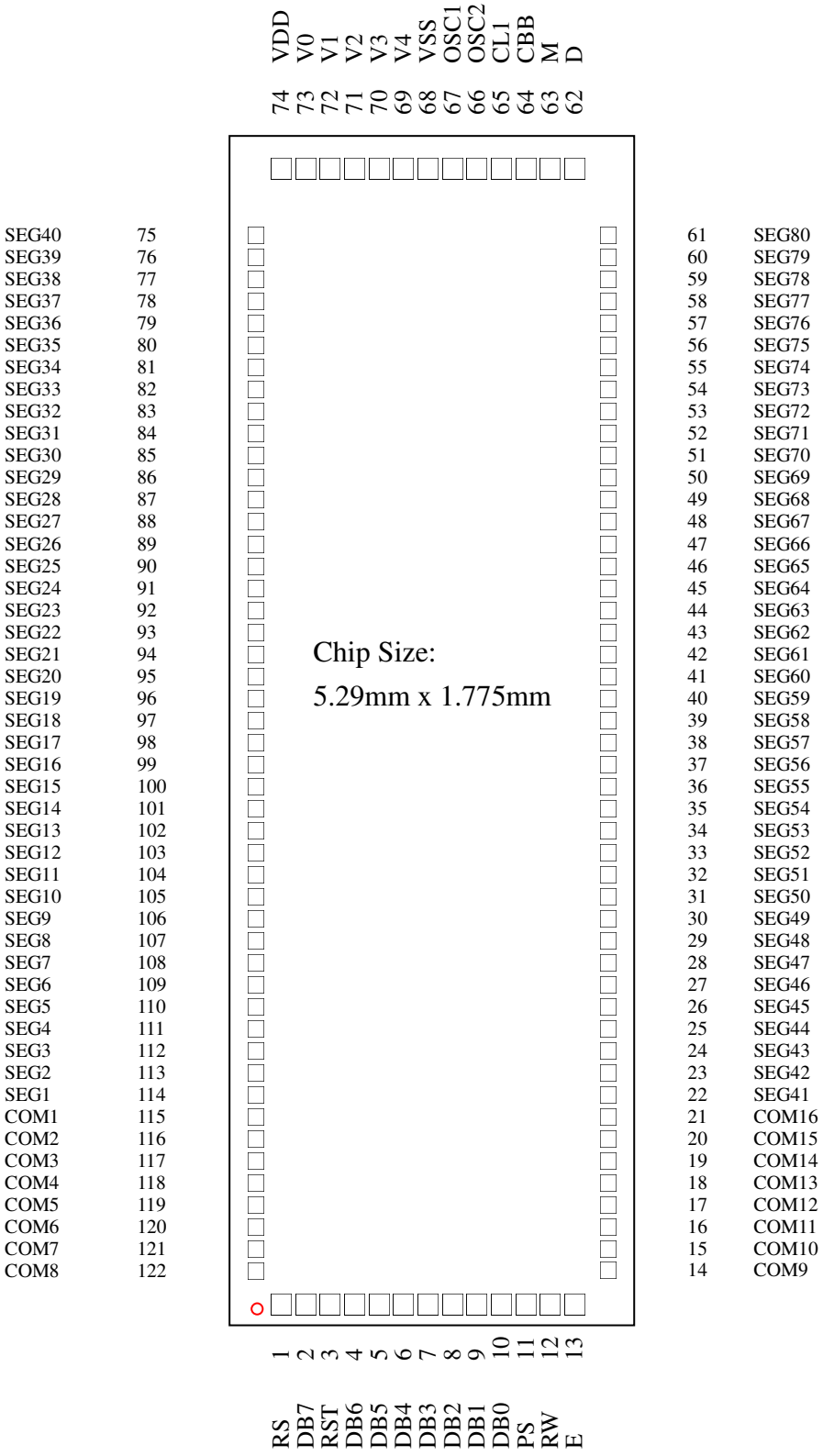


Figure 1. SA8016 block diagram

Pad Diagram



Substrate must connect to Vss or floating

Pad Location

No.	Name	X	Y
1	RS	59.0	1505.0
2	DB7	59.0	1395.0
3	RST	59.0	1285.0
4	DB6	59.0	1175.0
5	DB5	59.0	1065.0
6	DB4	59.0	955.0
7	DB3	59.0	845.0
8	DB2	59.0	735.0
9	DB1	59.0	625.0
10	DB0	59.0	515.0
11	PS	59.0	405.0
12	RW	59.0	295.0
13	E	59.0	185.0
14	COM9	265.0	59.0
15	COM10	355.0	59.0
16	COM11	445.0	59.0
17	COM12	535.0	59.0
18	COM13	625.0	59.0
19	COM14	715.0	59.0
20	COM15	805.0	59.0
21	COM16	895.0	59.0
22	SEG41	985.0	59.0
23	SEG42	1075.0	59.0
24	SEG43	1165.0	59.0
25	SEG44	1255.0	59.0
26	SEG45	1345.0	59.0
27	SEG46	1435.0	59.0
28	SEG47	1525.0	59.0
29	SEG48	1615.0	59.0
30	SEG49	1705.0	59.0
31	SEG50	1795.0	59.0
32	SEG51	1885.0	59.0
33	SEG52	1975.0	59.0
34	SEG53	2065.0	59.0
35	SEG54	2155.0	59.0
36	SEG55	2245.0	59.0
37	SEG56	2335.0	59.0
38	SEG57	2425.0	59.0
39	SEG58	2515.0	59.0
40	SEG59	2605.0	59.0
41	SEG60	2695.0	59.0
42	SEG61	2785.0	59.0

No.	Name	X	Y
43	SEG62	2875.0	59.0
44	SEG63	2965.0	59.0
45	SEG64	3055.0	59.0
46	SEG65	3145.0	59.0
47	SEG66	3235.0	59.0
48	SEG67	3325.0	59.0
49	SEG68	3415.0	59.0
50	SEG69	3505.0	59.0
51	SEG70	3595.0	59.0
52	SEG71	3685.0	59.0
53	SEG72	3775.0	59.0
54	SEG73	3865.0	59.0
55	SEG74	3955.0	59.0
56	SEG75	4045.0	59.0
57	SEG76	4135.0	59.0
58	SEG77	4225.0	59.0
59	SEG78	4315.0	59.0
60	SEG79	4405.0	59.0
61	SEG80	4495.0	59.0
62	D	5146.5	185.0
63	M	5146.5	295.0
64	CBB	5146.5	405.0
65	CL1	5146.5	515.0
66	OSC2	5146.5	625.0
67	OSC1	5146.5	735.0
68	VSS	5146.5	845.0
69	V4	5146.5	955.0
70	V3	5146.5	1065.0
71	V2	5146.5	1175.0
72	V1	5146.5	1285.0
73	V0	5146.5	1395.0
74	VDD	5146.5	1505.0
75	SEG40	4495.0	1631.0
76	SEG39	4405.0	1631.0
77	SEG38	4315.0	1631.0
78	SEG37	4225.0	1631.0
79	SEG36	4135.0	1631.0
80	SEG35	4045.0	1631.0
81	SEG34	3955.0	1631.0
82	SEG33	3865.0	1631.0
83	SEG32	3775.0	1631.0
84	SEG31	3685.0	1631.0

No.	Name	X	Y
85	SEG30	3595.0	1631.0
86	SEG29	3505.0	1631.0
87	SEG28	3415.0	1631.0
88	SEG27	3325.0	1631.0
89	SEG26	3235.0	1631.0
90	SEG25	3145.0	1631.0
91	SEG24	3055.0	1631.0
92	SEG23	2965.0	1631.0
93	SEG22	2875.0	1631.0
94	SEG21	2785.0	1631.0
95	SEG20	2695.0	1631.0
96	SEG19	2605.0	1631.0
97	SEG18	2515.0	1631.0
98	SEG17	2425.0	1631.0
99	SEG16	2335.0	1631.0
100	SEG15	2245.0	1631.0
101	SEG14	2155.0	1631.0
102	SEG13	2065.0	1631.0
103	SEG12	1975.0	1631.0
104	SEG11	1885.0	1631.0
105	SEG10	1795.0	1631.0
106	SEG9	1705.0	1631.0
107	SEG8	1615.0	1631.0
108	SEG7	1525.0	1631.0
109	SEG6	1435.0	1631.0
110	SEG5	1345.0	1631.0
111	SEG4	1255.0	1631.0
112	SEG3	1165.0	1631.0
113	SEG2	1075.0	1631.0
114	SEG1	985.0	1631.0
115	COM1	895.0	1631.0
116	COM2	805.0	1631.0
117	COM3	715.0	1631.0
118	COM4	625.0	1631.0
119	COM5	535.0	1631.0
120	COM6	445.0	1631.0
121	COM7	355.0	1631.0
122	COM8	265.0	1631.0

Pin Description

Pin Name	Type	Function
VDD	Input	Positive voltage for logic circuit and LCD drivers
VSS	Input	Ground (0V)
V0, V1, V2, V3, V4	Input	Bias voltage level for LCD driving from the voltage divider: $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{SS}$ ($V0 - V_{SS} = 5V_{(Max.)}$)
COM1 - COM16	Output	Common signal outputs for LCD
SEG1 – SEG80	Output	Segment (information) outputs for LCD
OSC1, OSC2	-	OSC1 and OSC2 are connected to resistor for internal oscillator. If external oscillator is used, connect it to OSC1.
CLK1	Output	Clock signal for the data latch-up in the output registers of the extension drivers.
CBB	Output	Charge bump of booster.
M	Output	The alternating signal to change voltage polarity between outputs COM and SEG.
D	Output	Output of the serial data for the extension drivers
RS	Input	Signal for selection of an interface register. 1 = Data register for read and write 0 = Instruction register for write or the Busy flag for address counter (for read).
RW	Input	Selection of the reading/writing mode. 1 = read; 0 = write
E	Input	MPU interface operations enable.
DB0 - DB3	Input/Output	Lower 4 bit data of the MPU bi-directional interface in 8-bit mode. Not used in 4-bit mode and serial mode, must pull high not floating.
DB4 - DB7	Input/Output	Higher 4 bit data of the MPU bi-directional interface in 8-bit mode. DB7 used for Read of the Busy flag. Serial: DB7: data input pin for serial mode (SID) DB6: serial clock input for serial mode (SCLK) DB5: chip select pin for serial mode (CS) When serial interface, D4 pull high not floating.
PS	Input	Parallel or Serial select pin. 1 = Parallel, 0 = Serial
RST	Input	Hardware reset pin, Low active.

Functional Description of SA8016

1. General principles of operation

In SA8016 integrates all functions, needed for display of alphanumeric characters on the LCD screen: MPU system interface, display data memory, CGRAM and CGROM, LCD drivers for larger number of characters. This controller allows to builds the LCD module with minimum of external components.

The SA8016 is controlled by instructions from MPU interface. The interface contains 8-bit data bus DB [7.0], interface operation enable pin (E), read/write mode pin (RW), data register (DR) or instruction register select (IR) pin. An interface can to operate by two ways:

- 8-bit interface use all data bus and 3 mode control signals (totally 11 interface signals);
- 4-bit interface use high order 4-bit data bus (totally 7 interface signals), at that the transfer of the data and instruction byte is implemented twice (two E pulses). For the reliability increase of the operation of 4-bit interface the special synchronization for the data quadruples, allowing avoid the distortion of the received information.

The controller is operated through 2 input buffer registers: Instruction Register (IR) and Data Register (DR). The instructions and data are written into the selected register with E falling edge and then an interface is locked out for given instruction execution time. An instruction is decoded and implemented by controller according to an internal timing diagram independently of interface functioning. Busy Flag (BF) is used to check the state of the current instruction execution that MPU can to read in the “Busy Flag and address reading” mode. Before sending the MPU next instruction, MPU must make sure, that previous instruction is finished and the input registers are open for writing new data.

This interface construction allows operate with MPU high-frequency system bus independently from slow internal timing diagram of controller, forming the internal cycles of instructions executing, memory access and information refreshing on the screen.

Each instruction execution is accompanied with data reading from internal memory on the current address into output Data Register (DR). MPU can read this data by next Data Read instruction.

The controller has the wide instructions set:

- Control instruction by display and an information displaying (Display Clear, Cursor on / off)
- Instructions of address installation and control by the cursor and information location on screen (Cursor/display shift, DDRAM/CGRAM address setting, Reset);
- Instructions for the data writing in memory or for the data reading from memory;
- Instructions for the control by the controller operation modes (Setting of the operation state, setting of the data input mode).

The controller contains 3 memory units:

- DDDRAM: contains codes of the characters, displayed on the screen. The character order in DDRAM correspond to the character order their displaying on the screen (without taking account the display shift);
- CGROM – mask ROM of characters generator, CGROM consist of bank had 496s 5x8 characters.
- CGRAM - character generator RAM with the 64-byte capacity, in which the user can to write own pattern from program (altogether 8 characters of 5x8 format).

The controller memory (DDRAM or CGRAM) is addressed through an Address Counter (AC). It is necessary to use an instruction to define an address in the address counter. After execution of any read/write instruction, AC address automatically changes by 1. The direction of AC address change depends on the “ID” control bit of the “input data mode set” instruction. Besides the DDRAM current address, the Address Counter also defines the text cursor position on the LCD screen.

The controller has a function in which data write combines with display shift. When a character code written into the DRAM, the address automatically increment and the display shifts backward simultaneously. Visually the cursor remains in the same position and the input character line shifts backward. This mode is enabled by “S” control bit of the "Input data mode Set" instruction.

The automatic increment mode simplifies the controller programming.

DDRAM addressing depends on characters display mode on the screen. In 1-line mode, single address range from 0 up to 79 for all 80 characters is used. In 2-line mode DDRAM two ranges form address: from 0 up to 39 for the first line and from 64 up to 103 for the second line. There is no difficulty to notice that address high-order bit represent the line flag. When incrementing or decrementing of AC address counter, DDRAM address in series passes both ranges and accordingly the cursor moves from the first line to the second and vice versa. In large font characters mode the addresses also divided on two ranges: from 0 up to 39 are written the text line characters codes, and in the 64-103 ranges is coded information for the icons display.

The controller block diagram can be divided conditionally into the following sub-systems:

Logic control sub-system:

- MPU interface,
- Current address counter (cursor position),
- Controller clock signals and the time diagram generator,
- Timers for COM cycle cursor blinking,
- Cursor forming circuit,
- Power-on reset circuit,
- Instructions decoder.

Memory with the control circuits sub-system:

- Display data RAM (DDRAM),
- Character generator RAM (CGRAM),
- Character generator ROM (CGROM)

LCD driver sub-system with the control circuits and voltage level conversion circuit:

- COM counter & decoder
- COM drivers,
- SEG shift register and latches,
- SEG drivers,
- VLCD voltage divider and level shift circuit

2. Logic control sub-system

2.1. MPU interface

Interface registers

The SA8016 controller has two interface registers: instruction register (IR) and data register (DR). An instruction register – is write only and accepts an instruction code from the data bus. The data register is both read and write. The data exchange between the registers and MPU is performed through bi-directional Data Bus (DB) of MPU interface.

The registers are selected by RS (Register Selector) signal and read/write operations are implemented by RW (Read-Write) signal according to table 1.

The IR register is used for an instruction code store while instruction executing.

The DRin register is used for the temporary storage of data to be information write to DDRAM or CGRAM.

Table 1 Registers interface selection

RS	RW	Operation
0	0	Instruction writing into IR
0	1	Reading of Busy Flag (DB7) and Address Counter (DB6-DB0)
1	0	Data writing into DR
1	1	Data reading from DR

While executing any instruction RAM (DDRAM or CGRAM) data always is read automatically and the DR register always contains data from the last address (even if the address was changed during instruction execution). During the next read instruction implementation these data can be read through MPU interface. Thus it is guaranteed that MPU always will receive data from the last address.

The general destination of the interface registers is the separation of the MPU interface-timing diagram from an internal controller-timing diagram. The controller operation is realized according to an internal timing diagram, which is clocked by the sufficiently low frequency of the clock generator. The IR and DR registers allow rapidly the data to write and read, released the MPU data bus during the instruction execution.

Busy Flag (BF)

Before writing the next instruction, MPU must ensure that previous instruction is completed and interface registers are free. To do this, MPU can check the Busy Flag (BF). If Busy Flag = 1, the controller is executing the previous instruction and MPU must perform idle cycles or other operations to wait for the busy flag to go to 0 state.

Busy Flag is read when RS=0 and RW=1 at DB7 output (see Table 1). The BF read procedure and current address is used only to check the controller current state and is not an instruction, therefore it does not lock input registers.

4-and 8-bit interface

SA8016 controller can operate with 4 or 8- bit data bus interface with MPU. The 4-bit, 8-bit interface choice is made by “Functional state setting” instruction.

- In 8-bit mode of the bit interface all 8 bits of the data bus are used. The data are strobe by the falling edge of E signal. On the falling edge of the E signal an instruction execution is started and Busy Flag (BF) is set to “1” (see Figure 2).
- In the 4-bit interface mode, DB4-DB7 is used for information exchange with MPU. DB0-DB3 bits are not used. The 8-bit instructions and data are transmitted through the 4-bit interface in two passes. Accordingly two E pulses are needed (see Figure.3). Firstly 4 high order bits are transferred and then 4 low order bits. An internal controller data selector multiplexes the high or low tetrad of this register, switching on E signal falling edge. The instruction is completed on the second E pulse and accordingly Busy Flag is set to “1” only on falling edge of second E pulse.

Two E pulses should accompany each instruction. If this condition is violated, the sequence of data will be broken; thereof the high and low data tetrads in the controller registers exchange their places. Missing any one of the two E pulses, owing to MPU synchronization loss or noise influence will break all further functioning of the controller, since the instructions transfer is disrupted, the processor can be lose Busy Flag and so on.

To prevent this situation, the controller has the interface synchronization function, which provide the correct order of the data following in 4-bit interface: any change of both RS as well as RW signals reset the data selector to the initial state (see Figure 3). In other words the any change of the interface operation mode (even Busy Flag check) automatically set it in initial state. On the other hand, it is forbidden to change RS and RW state between E pulses during submission of single instruction.

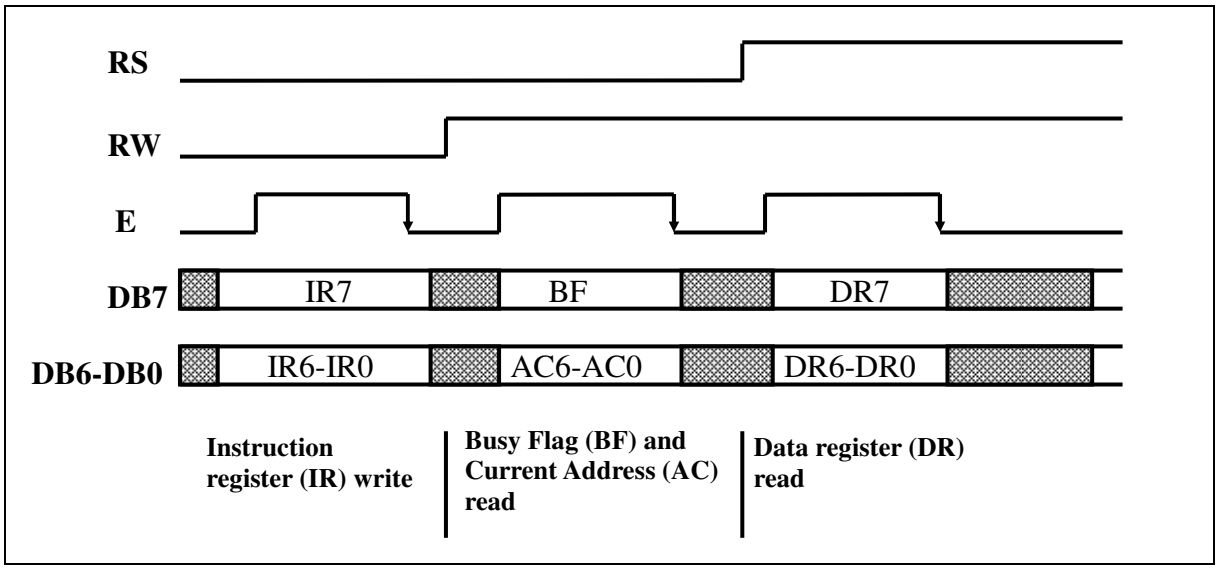
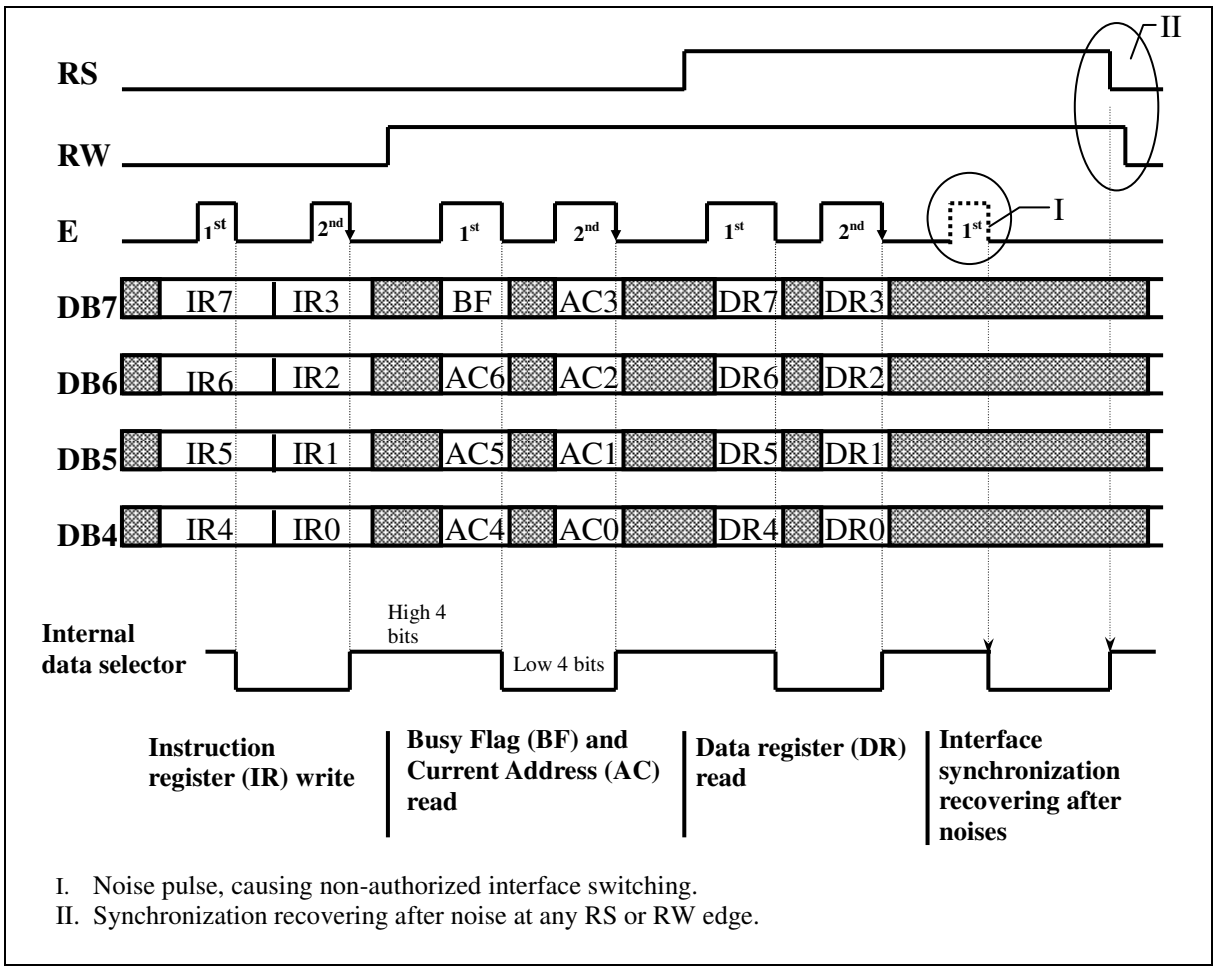


Figure 2. Example of 8-bit interface operation.



I. Noise pulse, causing non-authorized interface switching.
II. Synchronization recovering after noise at any RS or RW edge.

Figure 3. Example of 4-bit interface operation.

2.2. DDRAM address distribution

The controller can display the characters in one or two lines. The suitable mode is set by "Function set" instruction.

In one-line mode the controller display the 5x8 characters in single DDRAM addresses range from 0 up to 79 (4FH). COM [1...8] lines are used for 5x8 characters.

In two-line mode the controller display the 5x8 characters in two lines accordingly:

DDRAM addresses range from 0 up to 39 (27H) for the first line (COM [1...8]),

DDRAM addresses range from 64 (40H) up to 103 (67H) for the second line (COM [9...16]).

The correspondence between DDRAM addresses and character positions on display in one-line mode and also an example of cursor display in current display position, are shown in Figure 4.

The correspondence between DDRAM addresses and the character positions on display in two-line mode and also an example of cursor display in display position, are shown in Figure 6.

2.3. Current address counter

The current address, on which is implemented an access to the memory (DDRAM and CGRAM), and also determined the cursor position on display, are determined by Current Address Counter (AC). The counter has the functions of clearing in 0 state, setting of specified state, incrementing and decrementing.

AC reset to 0 is realized by "Display Clear" and "Return Home" instructions.

The set of AC random address is implemented by "Address DDRAM Set" and "Address CGRAM Set" instructions. In this case the new address is written in AC from Instruction register (IR). By these instructions is also determined the memory type, to which are following accesses.

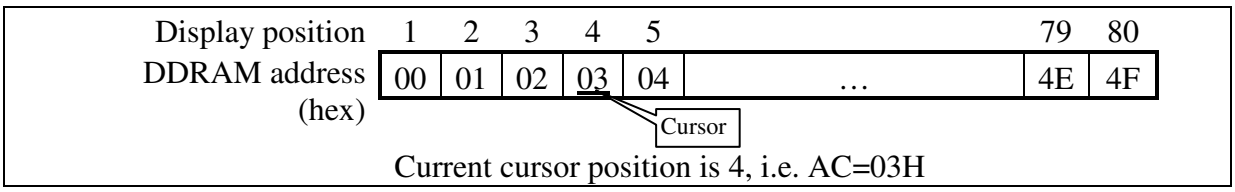


Figure 4.: One-line display without shifting.

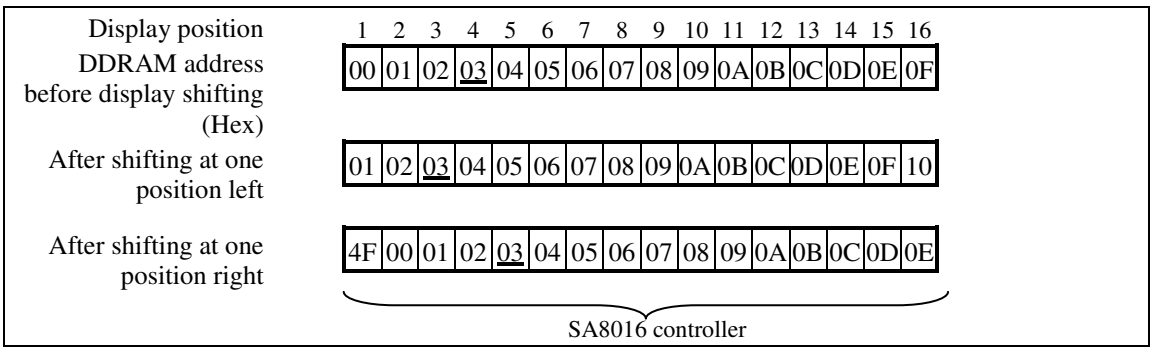


Figure 5.: Display shifting in one-line mode.

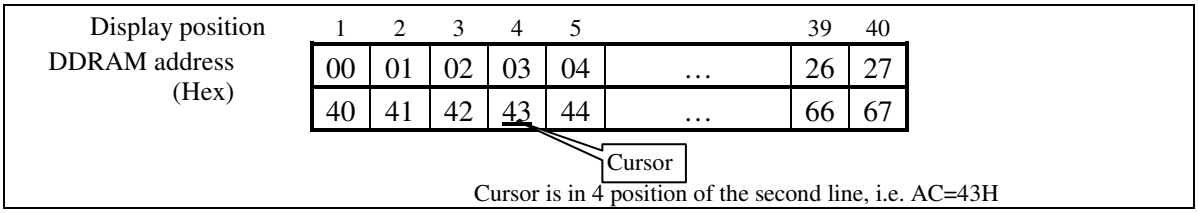


Figure 6.: 2-line display without shifting.

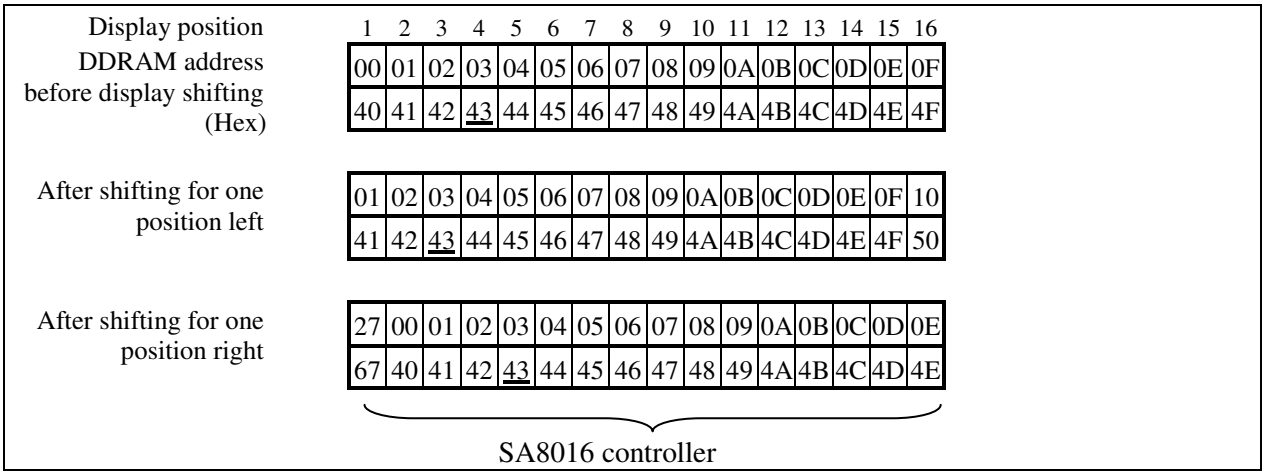


Figure 7. Display shift in 2-line mode.

An incrementing or decrementing of the AC address can made by following instructions:

- Memory read/write operation. The count direction is determined by “ID” bit of “Input data mode set” (see part “Instruction description”).
- Cursor shift, in which also the direction count is determined.

The count order of AC address depends from the displaying characters format, the number of the display lines and from the memory type, to which an access is implemented (DDRAM or CGRAM).

While access to CGRAM the AC counter operate as complete 7-bit reversible counter without count limitations.

When access to DDRAM, the count order is following:

- For one-line mode:
  - Incrementing: 0, 1, 2, … 78, 79, 0, 1, 2…
  - Decrementing: 0, 79, 78, 77, … 2, 1, 0, 79…
  - At the setting of the random address more than 79, the counter is incremented up to 127 and then set to 0.
- For two-line mode:
  - Incrementing: 0, 1, 2, … 38, 39, 0, 1, …
  - Decrementing: 0, 103, 102, … 65, 64, 39, 38, … 2, 1, 0, 103, …

At the setting of the random address more than 103, the counter is incremented up to 127 and then set to 0.

Character Code (DDRAM Data)									CGRAM Address						Character Patterns (CGRAM Data)							
B8	B7	B6	B5	B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	-	0	0	0	0	0	0	0	0	0	-	-	-	0	1	1	1	1
						0	0	0				0	0	1				1	0	0	0	0
						0	0	0				0	1	0				1	0	0	0	0
						0	0	0				0	1	1				0	1	1	1	0
						0	0	0				1	0	0				0	0	0	0	1
						0	0	0				1	0	1				0	0	0	0	1
						0	0	0				1	1	0				1	1	1	1	0
						0	0	0				1	1	1				0	0	0	0	0
0	0	0	0	0	-	0	0	1	0	0	1	0	0	0	-	-	-	0	1	1	1	0
						0	0	1				0	0	1				1	0	0	0	1
						0	0	1				0	1	0				1	0	0	0	1
						0	0	1				0	1	1				1	0	0	0	1
						0	0	1				1	0	0				1	1	1	1	1
						0	0	1				1	0	1				1	0	0	0	1
						0	0	1				1	1	0				1	0	0	0	1
						0	0	1				1	1	1				0	0	0	0	0

Table 2 Relationship between Character Code, CGRAM address and Character pattern

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical or with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 2, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

" - ": Indicates no effect.

Instruction table

Instruction	Instruction Code										Description	Description Time(270kHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
EXT = 0 or 1												
Display clear	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM and set DDRAM address to “00H” from AC	1.52ms
Return home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to “00H” from AC and return cursor to its orginal position if shifted. The contents of DDRAM are not changed.	0µs
Display On / Off	0	0	0	0	0	0	1	D	C	P	D=1: entire display on C=1: cursor on P: font table page selection	37µs
Cursor or display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit and direction, without changing DDRAM data.	37µs
Function Set	0	0	0	0	1	DL	N	EXT	x	x	DL: interface data 8/4 bits N: number of line 2/1	37µs
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contenets of address counter can also be read.	0µs
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into interanl RAM (DDRAM/CGRAM)	37µs
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	37µs
EXT = 0												
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Set cursor move direction and specifies display shift. These operations are performed during dat awrite and read.	37µs
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	37µs
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	37µs
EXT = 1												
Bias resistor select	0	0	0	0	0	0	0	1	Rb1	Rb0	Used internal resistor only provide 1/5 bias mode. Rb[1:0] = 00→ external resistor Rb[1:0] = 01 to 11→ internal resistor	37µs
COM, SEG direction select	0	0	0	1	0	0	C1	C2	S1	S2	C1:COM1~8→COM8~1 C2:COM9~16→COM16~9 S1:Seg1~40→Seg40~1 S2:Seg41~80→Seg80~41	37µs
Set display data length	0	0	1	L6	L5	L4	L3	L2	L1	L0	To specifiy the number of data bytes (3SPI mode)	37µs

Note: Be sure SA8016 in not in busy state (BF=0) befroe sending an instruction from MPU to SA8016. If instruction is sent without checking the busy flag, the time between the first instruction and next will take much longer than instruction time itself. Refer the instruction Table for the list of each instruction execution time.

Instruction Desciption

EXT = 0 or 1

Display Clear

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

The "Display Clear" instruction writes 20H code into all DDRAM addresses (in CGROM coding that must be the space code). Then an address counter (AC) and display shift counter are set in 00H state. In other words, an initialization of the display data and the display and cursor state take place. It also set the I/D bit of "data input mode" to "1" state; the S bit state does not change.

Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	x

The "Reset" instruction set AC address in 0, and also returns the display to its initial state, if it was shifted. The DDRAM contents do not change. The I/D bit of the "Data input mode" instruction set in "1", the S bit state do not change.

According to there settings the cursor returns in the first position of screen (in the first line, if display is in the two-line mode).

Display On / Off

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	P

D: Display On / Off control bit

The display is on when D=1 and off when D=0. At that, all written data are stored in memory, but at D=0 theirs are not displayed. The cursor and character blinking also are not displayed.

C: Cursor On / Off control bit

At C=0 the cursor off, at C=1 the cursor is on and displayed on the screen in position, corresponding to the AC.

P: Font table selection bit

At P=0, it select page 1 of font table (set DDRAM data bit 8 = 0)

At P=1, it select page 2 of font table (set DDRAM data bit 8 = 1)

Cursor or display shift

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	x	x

This instruction shift cursor or entire display to the left or to the right without changing of the memory contents (see Table 3). The cursor shift is represent the incrementing or the decrementing of the address counter (AC). The shift of an entire display represent the incrementing or the decrementing of the initial address counter at the screen refresh without changing of the AC state, as a result the cursor follow behind the display shift.

At the cursor shift in the two-line mode the cursor is moved from first line into second line and conversely according to the regulations of address count (AC) At the display shift in two-line mode the characters in each line are shifted parallel and not pass from one line in another (see Figure 3).

Table 3. Cursor and Display Shift modes

S/C	R/L	Description
0	0	Cursor shift to the left (AC is decremented by 1)
0	1	Cursor shift to the right (AC is incremented by 1)
1	0	Display shift to the left (start refresh address is incremented by 1)
1	1	Display shift to the right (start refresh address is decremented by 1)

Function set

The instruction is destined for the setting of the controller basic operation parameters setting. The destinations of the bit instruction depend from the characters displaying mode on the screen.

In standard mode:

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	EXT	x	x

DL: Interface data length control bit

At DL=0, it mean 4 bit bus mode with MPU.

At DL=1, it mean 8 bit bus mode with MPU.

N: Display line number control bit

At N=0, 1 line display mode is set.

At N=1, 2 lines display mode is set.

EXT: Select basic or extended instruction set

At EXT=0, the commands “Entry Mode Set”, “Set CGRAM address” and “Set DDRAM address” can be performed. (disable extension instruction)

At EXT=1, the commands “Bias resistor select”, “COM,SEG direction select” and “Set display data length” can be perfomed. Other commanded can be executed in both cases. (enable extension instruction)

Read Busy Flag and address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

The read procedure of Busy Flag (BF) and AC current address allow to determine the controller busy state during an execution of the current instruction. If BF=1, the controller is in the state of the instruction execution, therefore, the new instruction, given in this moment, will ignored. For the correct input of the next instruction MPU must to expect, when BF pass in 0 state.

Simultaneously with the BF reading on DB7 MPU become the address counter (AC) state on DB6-DB0. The AC address format coincides with the setting instructions of DDRAM/CGRAM address.

It should to have in view, that the AC address value can change during the implementation of some instructions (i.e. at BF=1), accompanied by the address change (for example, data read/write, cursor moving, display clear instructions etc.).

The writing procedure of Busy Flag is destined only for determination of the controller current state and is not the instruction, as do not change the controller state and do not require of an execution (execution time is 0).

Write Data to CGRAM or DDRAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

The instruction is write the 8-bit data in DDRAM or CGRAM to AC current address. The data destination selection for the writing in DDRAM or CGRAM is implemented by previous instruction of DDRAM or CGRAM address setting. After data writing the AC addresses are automatically incremented or decremented according to the ID bit state of the “Data input set mode” instruction. According with that occur the cursor shift on the display to the right or to the left. Also simultaneously with the data writing in DDRAM (but not in CGRAM!) it can occur the display shift in an opposite side, if it is enabled by S bit of “Data input mode set” previous instruction.

Read Data from CGRAM or DDRAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

It is an instruction for the reading of 8-bit data from DDRAM or CGRAM on the AC current address. The selection between DDRAM and CGRAM is realized by previous instruction of the setting of DDRAM address or CGRAM address.

The data reading procedure from memory is occurs in two stages. After any instruction execution DDRAM/CGRAM data is put into output data register. This is guaranteed that in output data register always will be contained the data of the current address, even if it was changed during the last instruction execution. At a time of the reading instruction execution at the E signal high level,

the data from the output register are transferred DB interface. And then at E fall edge occur the incrementing or decrementing of AC address according to the ID bit state of “Input data state mode”, and also the data reading on the AC new address from memory into the output register.

At the data reading the display shift is not occurs.

The automatic incrementing or decrementing of AC address bring, particularly, to the situation, when just now written data it is not possible at once to read, as the memory reading will be occur already on the new address. For it implementation it is necessary before reading to give the address or the cursor shift set instruction for the return of the AC previous value.

EXT=0

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	ID	S

I/D: incrementing (ID=1) or decrementing (ID=0) of the Address Counter (AC) when the data writing or reading in DDRAM or CGRAM. Accordingly, the cursor and the character blinking are shifted to the right at an incrementing and to the left at the decrementing.

S: Display shift enable to the left (ID=1) or to the right (ID=0) at S=1 during writing of the character code to DDRAM. At S=0 display shift is disabled. At an accessing to CGRAM the display shift is not occur and this bit state have not the significance.

When the display shift is enabled, it is occur simultaneously with the cursor shift, but it direction is in opposition to the cursor move direction. Thus, an effect is created, the cursor stay on the place, and entire display along with the setting character is moved in opposite direction.

Set CGRAM address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

The CGRAM address set instruction write CGRAM 6-bit address in the address counter (AC). It is simultaneously set the CGRAM access flag, as a result the following data write/read instructions will to direct theirs in CGRAM.

Set DDRAM address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

The DDRAM address set instruction write the DDRAM 7-bit address in the address counter (AC). It is simultaneously set the CGRAM access flag, as a result the following data write/read instructions will to direct theirs in DDRAM.

In the one-line display (N=0) for the DDRAM address must to 00H-4FH (0-79) range. In the two-lines display (N=1) for the DDRAM address must to 00H-27H (0-39) range for first line and in 40H-67H (64-103) range for second line.

EXT = 1

Bias resistor select

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	Rb1	Rb0

Set internal bias resistor vaule

Rb1	Rb0	Description
0	0	External bias resistor select
0	1	Built in resistor (2.2k ohm)
1	0	Built in resistor (6.8k ohm)
1	1	Built in resistor (9.0k ohm)

COM, SEG direction select

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	C1	C2	S1	S2

The SEG and COM output in SA8016 all have bi-direction control by the register.
COM output

C1	COM1		COM8
0	COM1	→ Common address →	COM8
1	COM8	→ Common address →	COM1

C2	COM9		COM16
0	COM9	→ Common address →	COM16
1	COM16	→ Common address →	COM9

SEG output

S1	SEG1		SEG40
0	SEG1	→ Segment address →	SEG40
1	SEG40	→ Segment address →	SEG1

S2	SEG41		SEG80
0	SEG41	→ Segment address →	SEG80
1	SEG80	→ Segment address →	SEG41

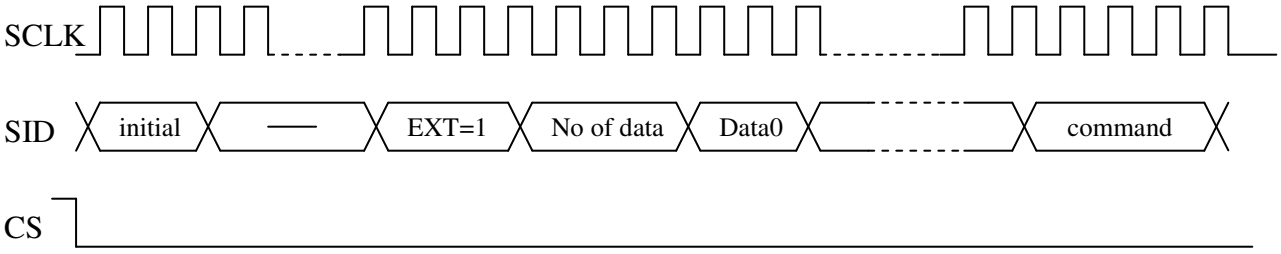
Set display data length

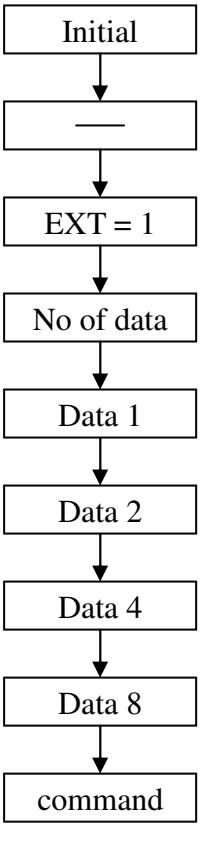
RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	L6	L5	L4	L3	L2	L1	L0

L6	L5	L4	L3	L2	L1	L0	Data length
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	79
1	0	0	1	1	1	1	80

Only in 3SPI interface will use the register to set the number of display data(max. 4F).

To write data to DDRAM, send Data Direction Command in 3 pin SPI. Data is latched at the rising edge of SCLK and DDRAM column address pointer will be increased by one automaticlly.





For example:

No of data = 01001000B

Data 1 = 00H (1st)

Data 2 = 01H (2nd)

Data 5 = 04H (4th)

Data 8 = 08H (last)

(*) This is command. 8 byte data is finished, so following data will be command

Reset Function

Initial by Internal Reset circuit

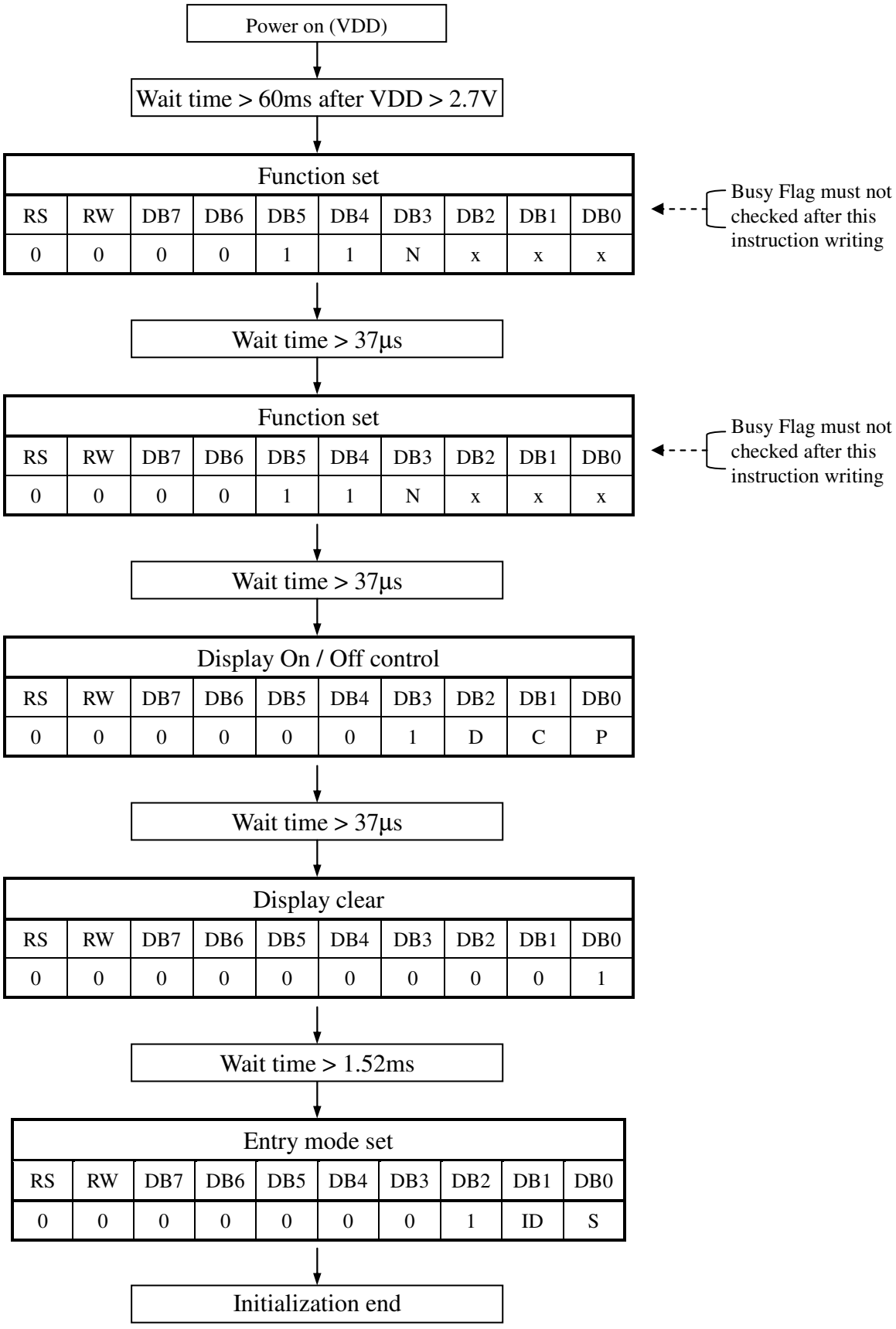
An internal reset circuit automatically initializes the SA8016when the power is turned on or hardware reset pin has low, The following instruction are executed during the initialization. The Busy flag(BF) is kept in the busy state until the initialization ends(BF = 1). The busy state lasts for 60ms after VDD rises to 2.7V.

1. Display clear
2. Function set
   DL = 1, 8 bit interface data
   N = 1, 2 line display
   EXT = 0, disable extension instruction
3. Display On / Off control
   D = 0, display off
   C = 0, cursor off
   P = 0, page 1 of font table (DDRAM data b8 = 0)
4. Entry mode set
   I/D = 1, increment by 1
   S = 0, no shift
5. Bias resistor select
   Rb1 = 0, Rb2 = 0 select external bias resistor
6. COM, SEG direction select
   C1, C2 =0, common not reverse
   S1, S2 = 0, segement not reverse

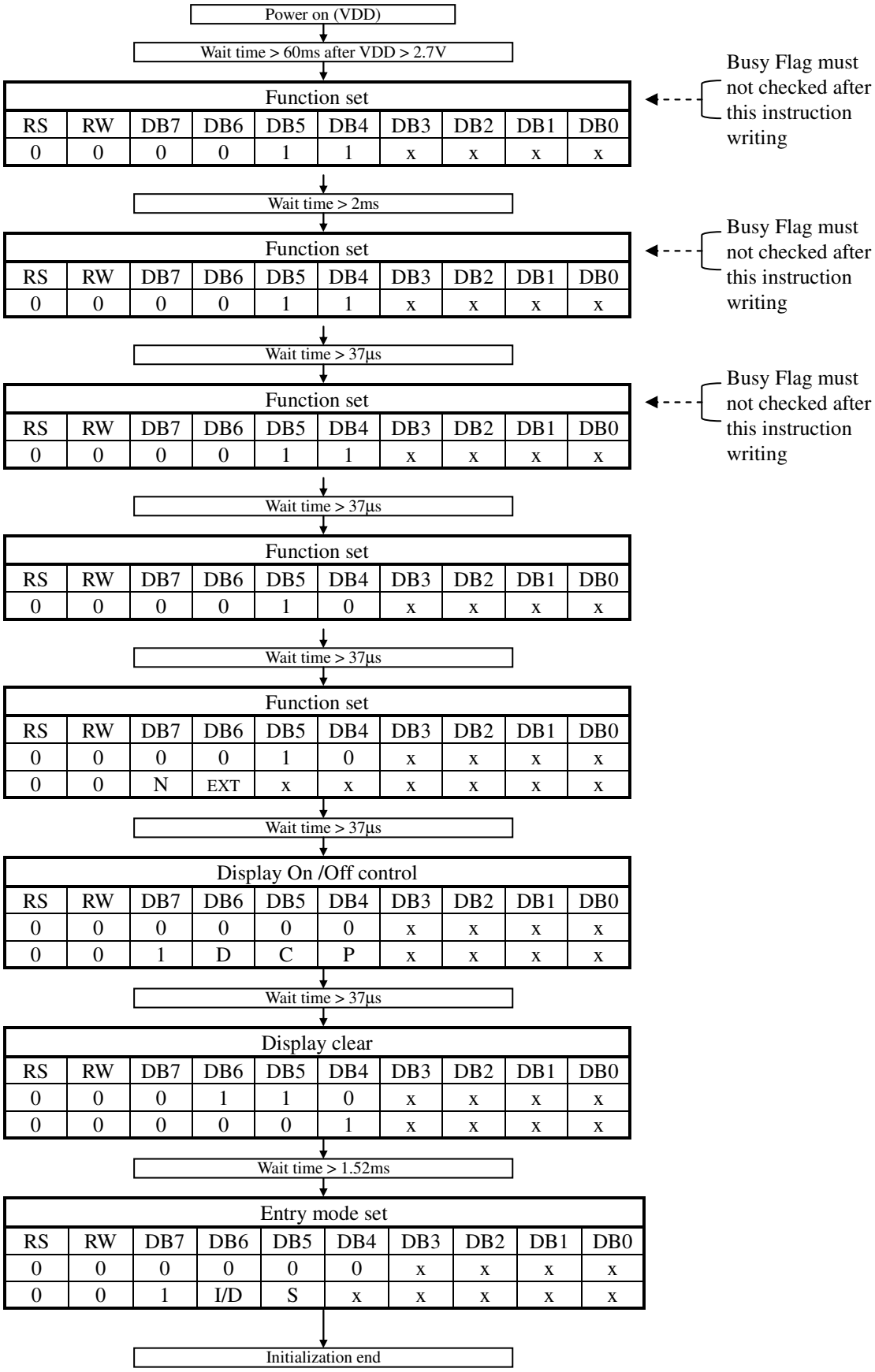
Note: If the electrical characteristics conditions listed under the table Power Supply Conditions. Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail ti initialize the SA8016. For such a case, initialization must be performed by the MPU as explain by the following figure.

Initializing by instruction

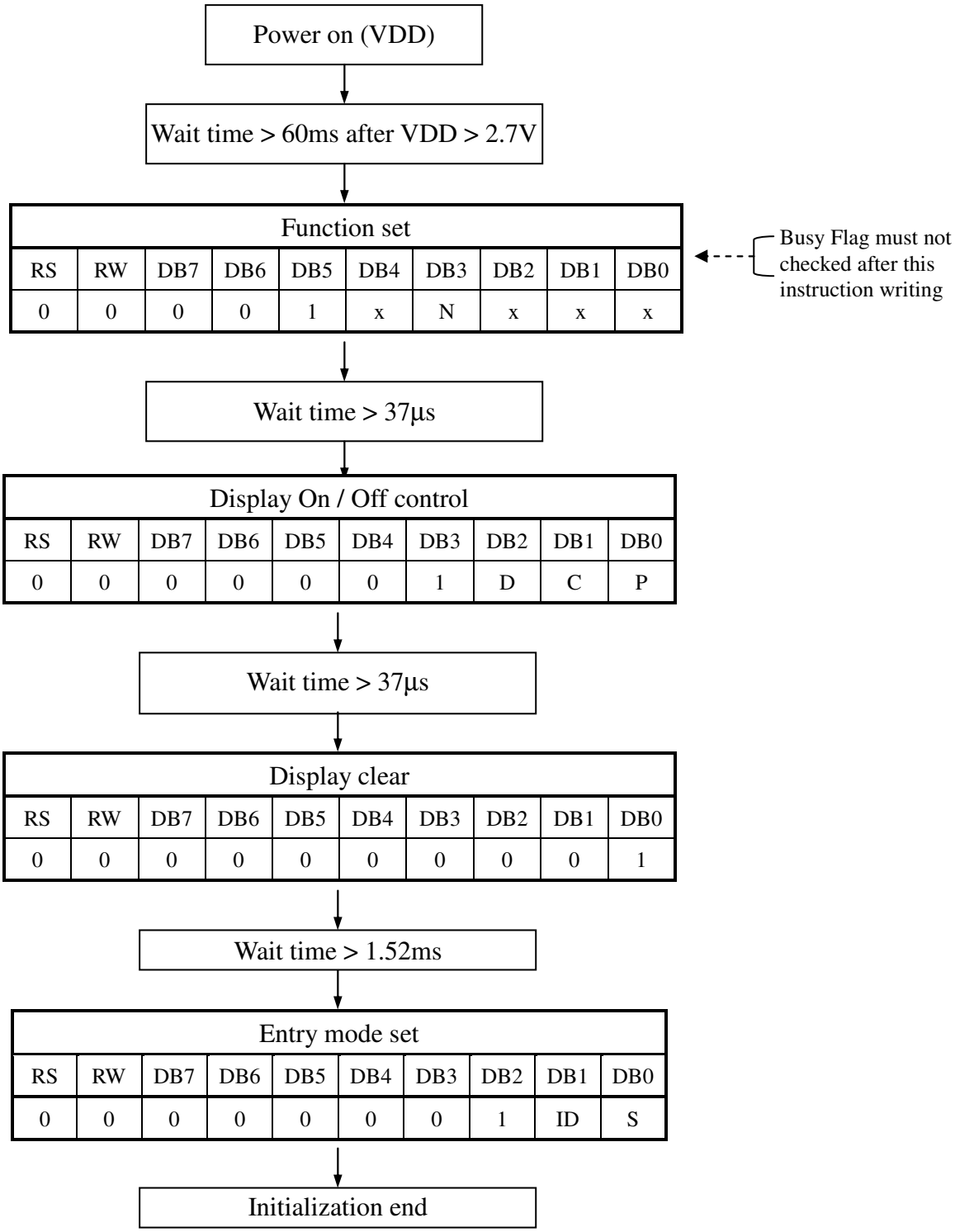
8 bit interface (fosc = 270kHz)



4 bit interface (fosc = 270kHz)



Serial Interface (fosc = 270kHz)

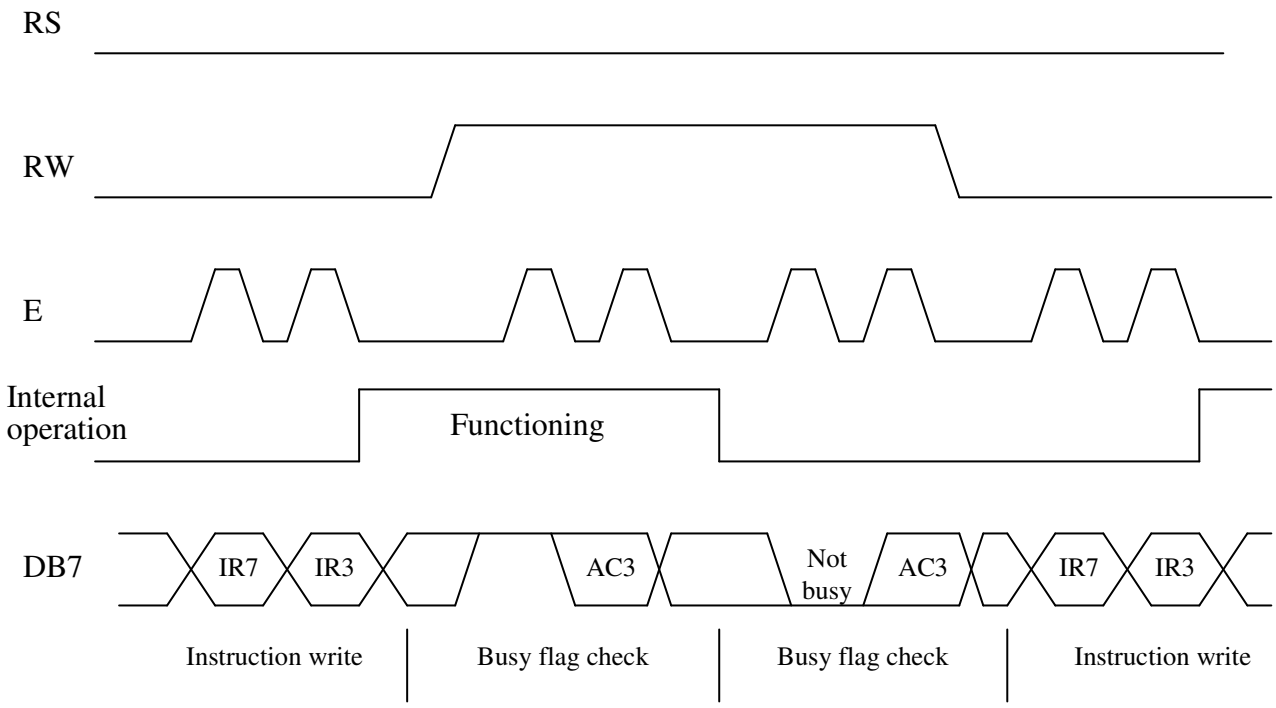


Interfacing to MPU

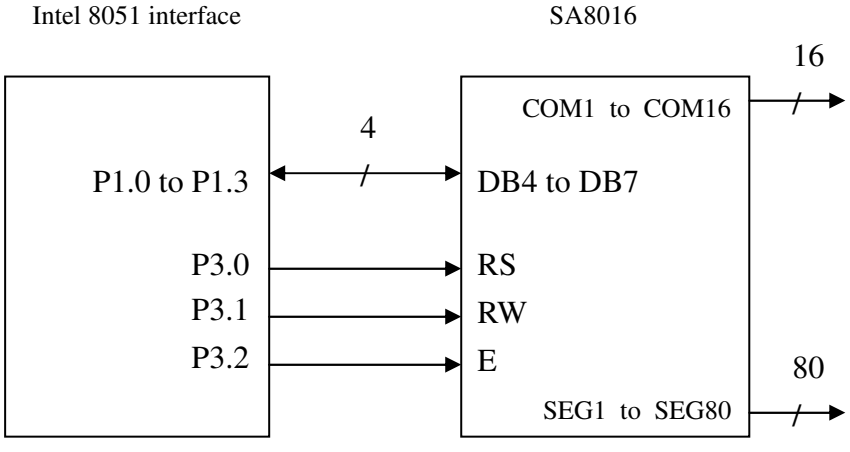
SA8016 can send data in ether two 4 bit , one 8 bit or serial operation, thus allowing interfacing with 4 or 8 bit or serial MPU.

For 4 bit interface data, only four bus lines (DB4 to DB7) are used for transfer. Bus lines DB3 to DB0 are disabled. The data transfer between SA8016 and MPU si completed after 4 bit data had been transferred twice. As for the order of data transfer, the four high order bits (for 8 bit operation, DB4 to DB7) are transferred before the four low order bits (for 8 bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4 bit data had been transferred twice. Two more 4 bit operation then transfer the busy flag and address counter data.

Example of busy flag check timing sequence

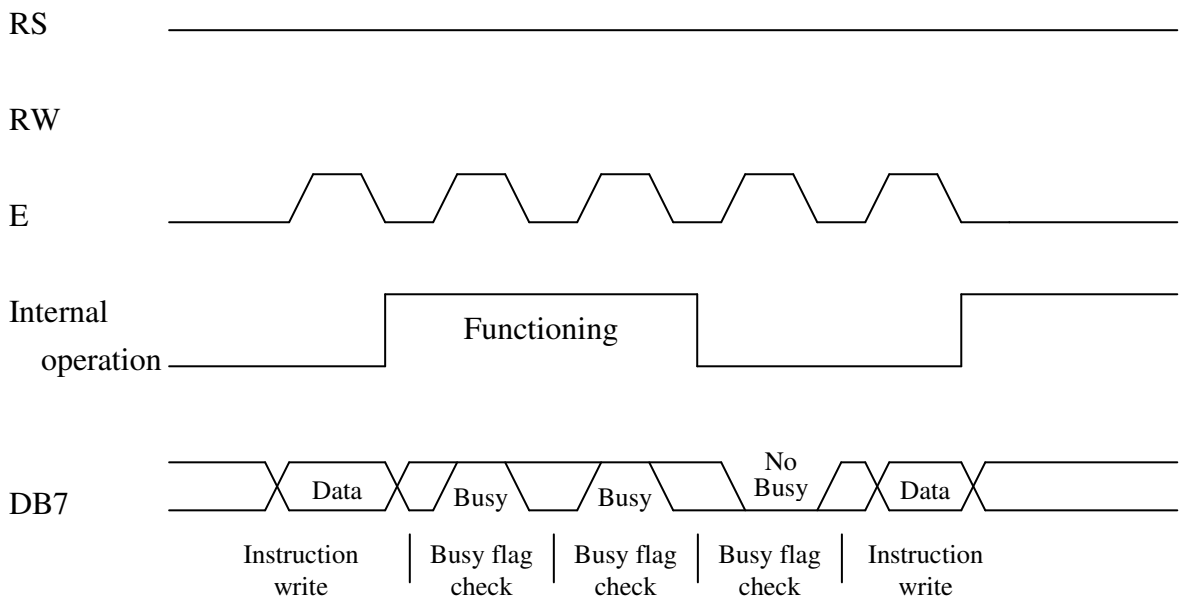


Intel 8051 interface

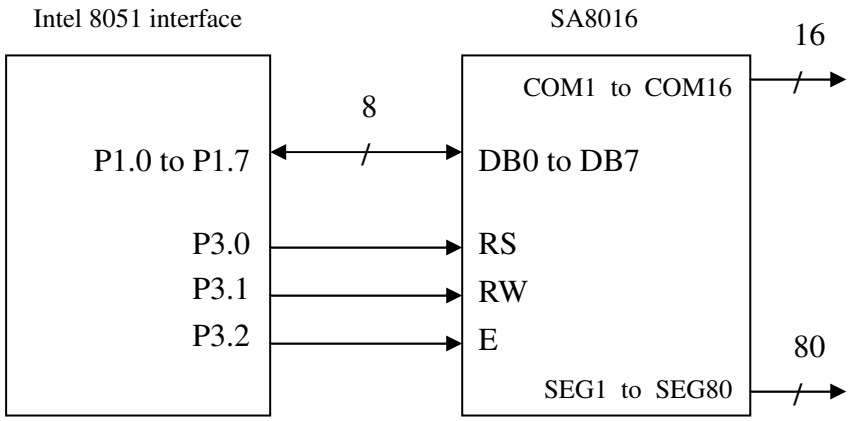


For 8 bit interface data, all eight-bus lines (DB0 to DB7) are used.

Example of busy flag check timing sequence

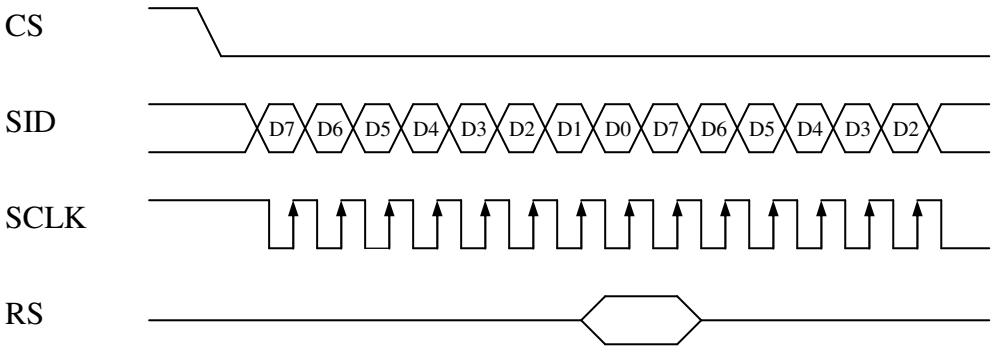


Intel 8051 interface

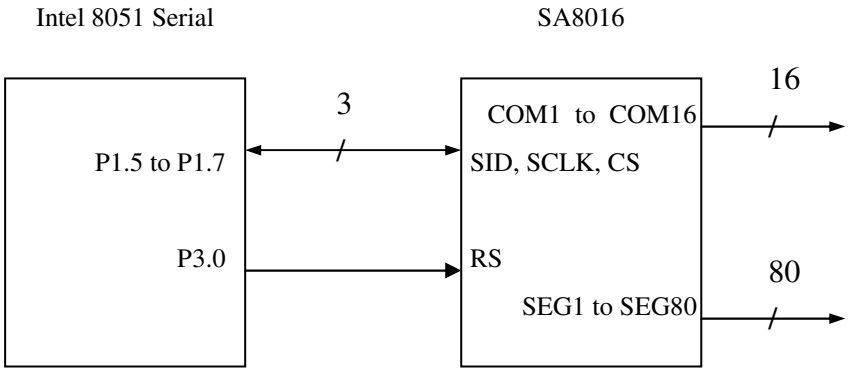


For serial interface data bus lines (DB5 to DB7) are used 4 pin SPI

Example of timing sequence

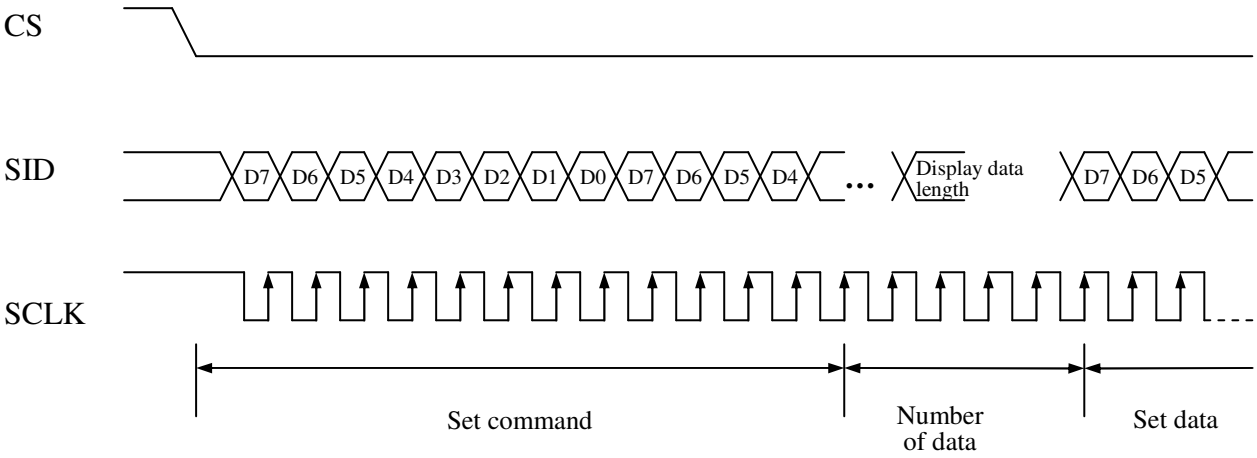


Intel 8051 interface (Serial)

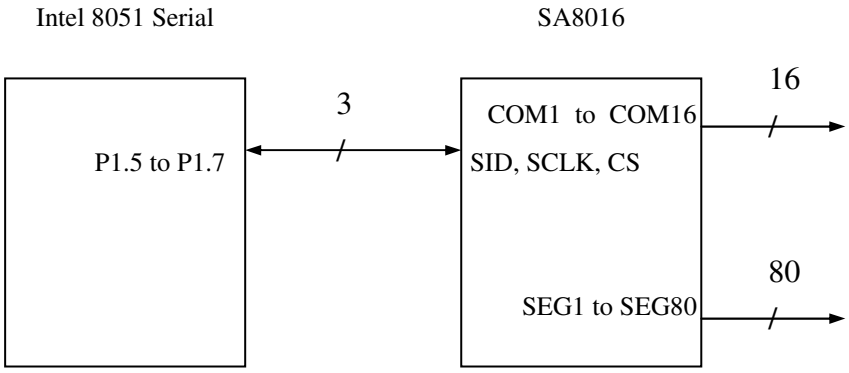


For serial interface data bus lines (DB5 to DB7) are used 3 pin SPI

Example of timing sequence



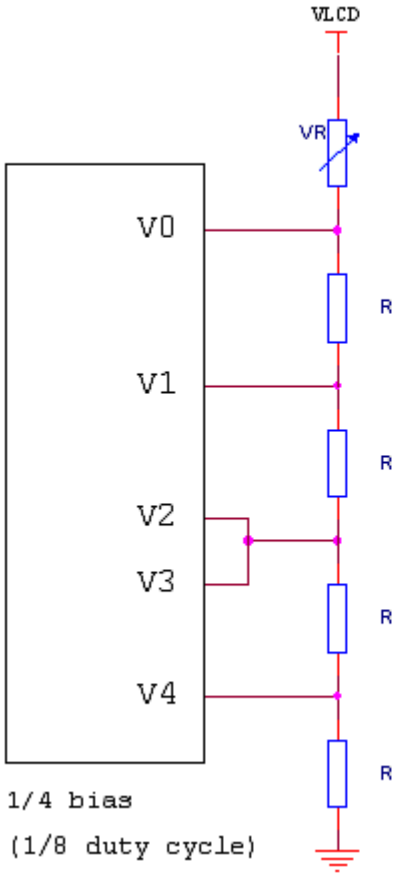
Intel 8051 interface (Serial)

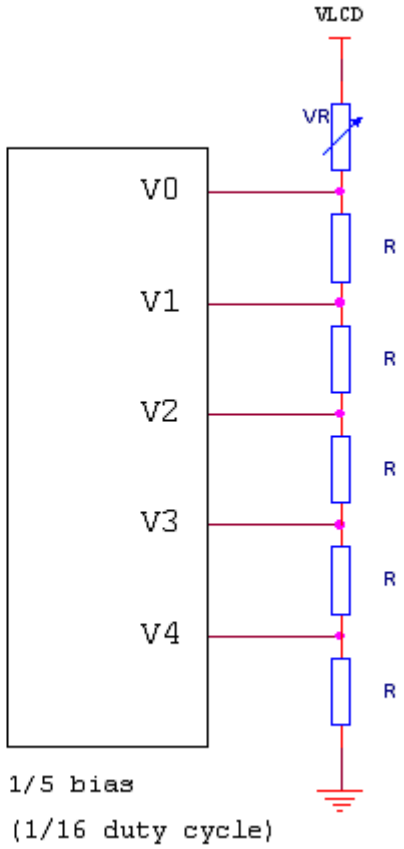


Supply voltage for LCD drive

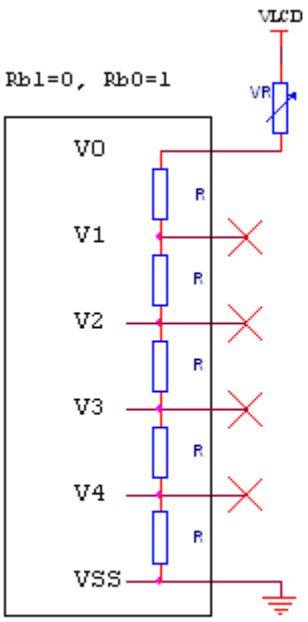
There are different voltages that supply to SA8016 pin (V0-V4) to obtain LCD drive waveform. We could use the register command (Rb1, Rb0) to set up the internal or external bias resistor. The relations of the bias, duty factor and supply voltages are shown as below. External bias resistor could setup to 1/4 and 1/5 bias, but internal bias resistor only could setup to 1/5 bias.

External Resistor	**Duty factor**	
	1/8	1/8, 1/16
	Bias	
Supply voltage	1/4	1/5
Bias resistor select	Rb1=0, Rb0=0	Rb1=0, Rb0=0
V0	V0	V0
V1	3/4 V0	4/5 V0
V2	1/2 V0	3/5 V0
V3	1/2 V0	2/5 V0
V4	1/4 V0	1/5 V0

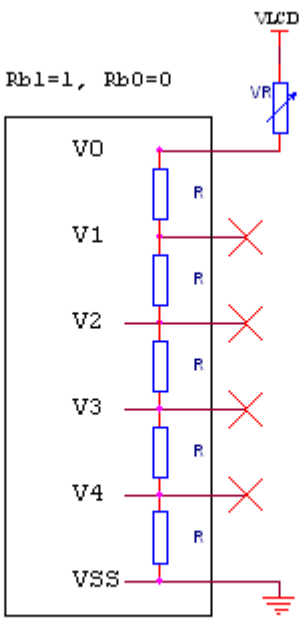




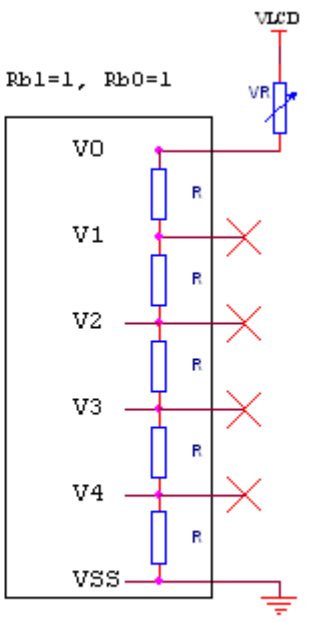
Internal resistor	Duty factor		
	1/8, 1/16		
	Bias		
Supply voltage	1/5	1/5	1/5
Bias resistor select	Rb1=0, Rb0=1	Rb1=1, Rb0=0	Rb1=1, Rb0=1
Internal resistor	R = 2.2k ohm	R = 6.6k ohm	R =9.0k ohm
V0	V0	V0	V0
V1	4/5 V0	4/5 V0	4/5 V0
V2	3/5 V0	3/5 V0	3/5 V0
V3	2/5 V0	2/5 V0	2/5 V0
V4	1/5 V0	1/5 V0	1/5 V0



1/5 bias, R=2.2k
(1/8, 1/16 duty cycle)



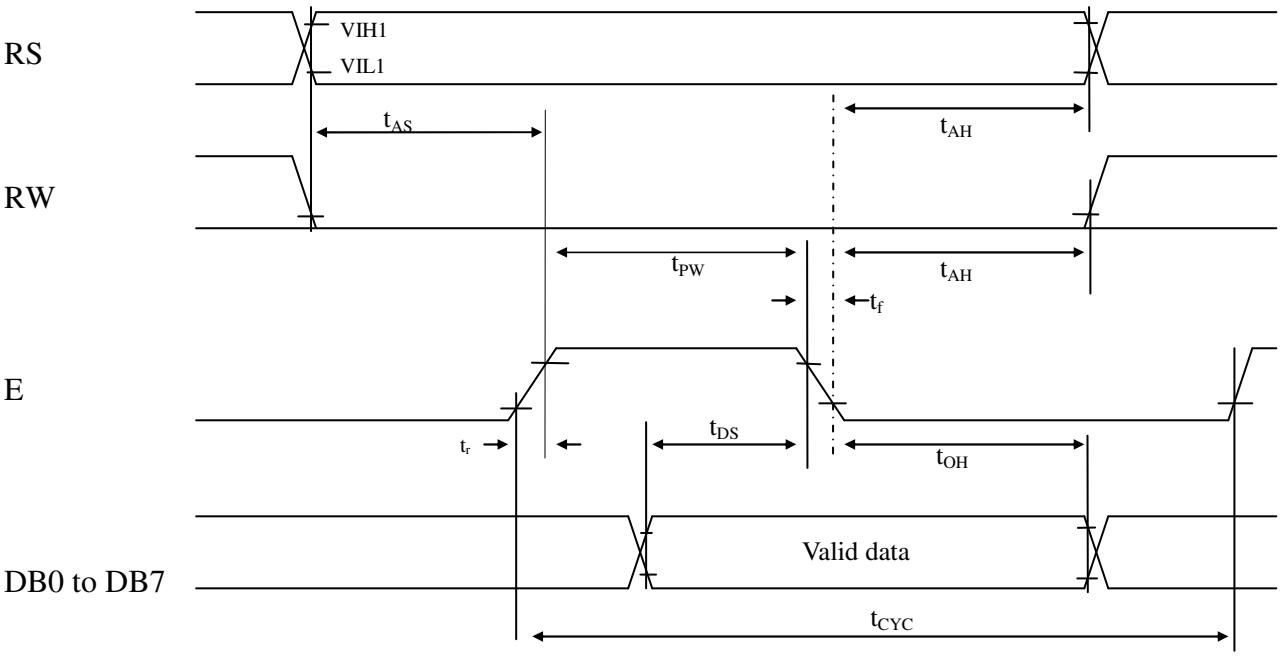
1/5 bias, R=6.8k
(1/8, 1/16 duty cycle)



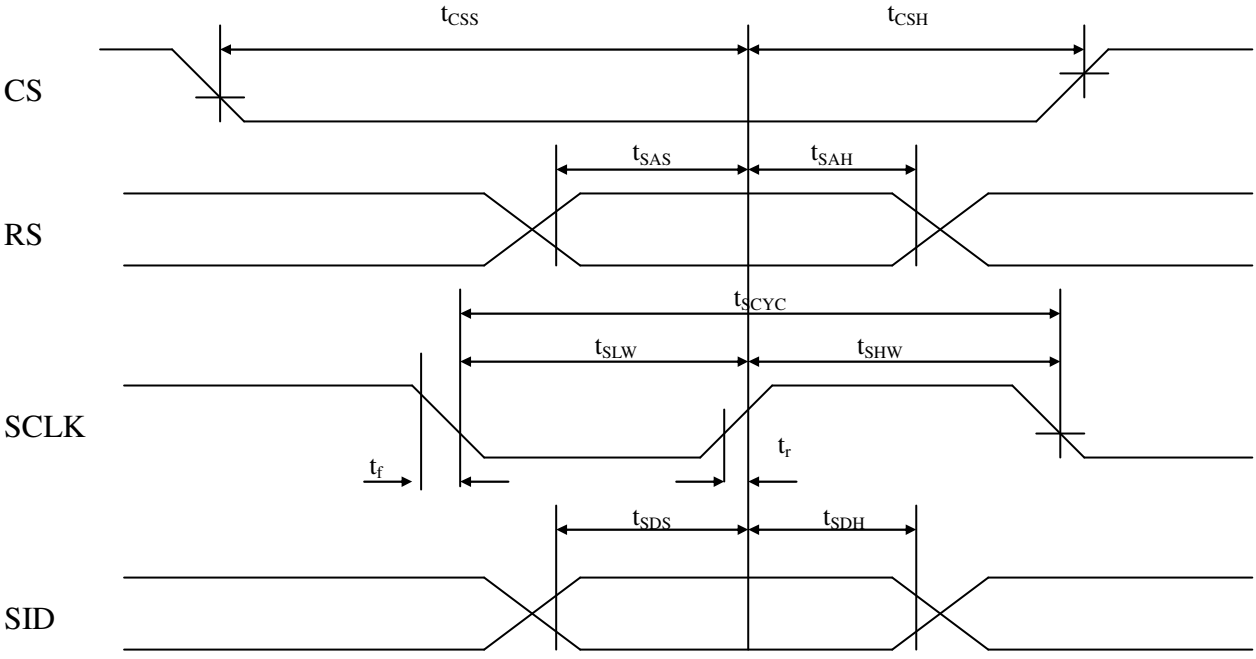
1/5 bias, R=9.0k
(1/8, 1/16 duty cycle)

Timing Characteristics

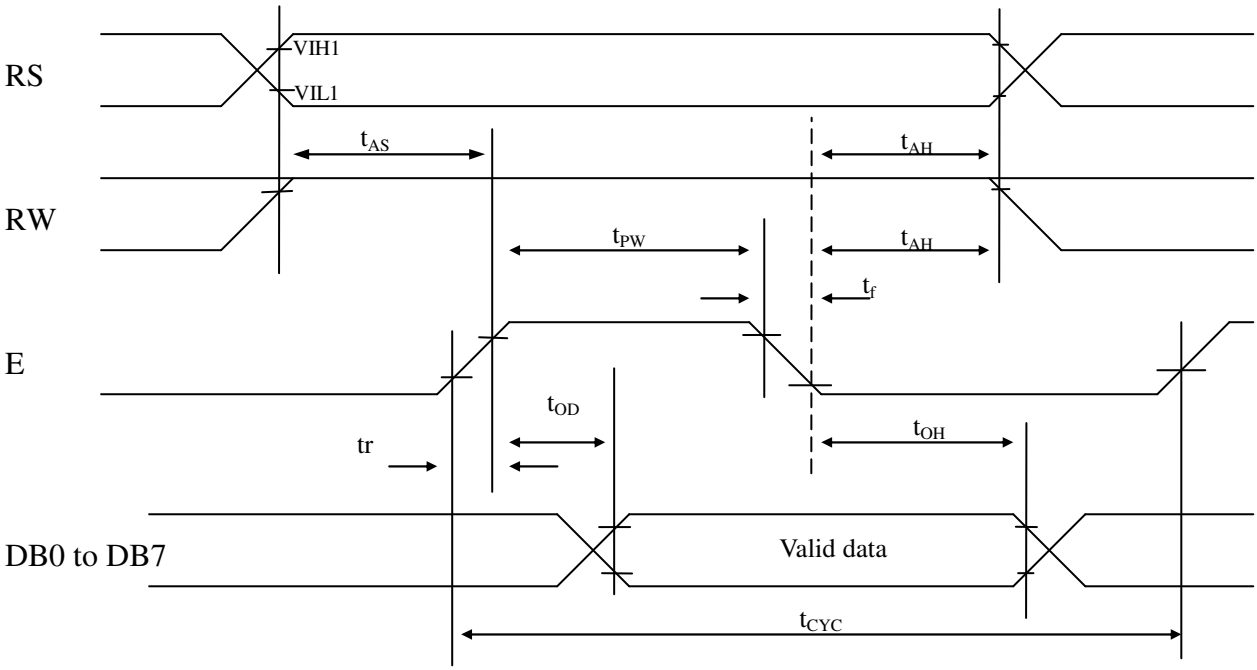
Writing data from MPU to SA8016 (Parallel)



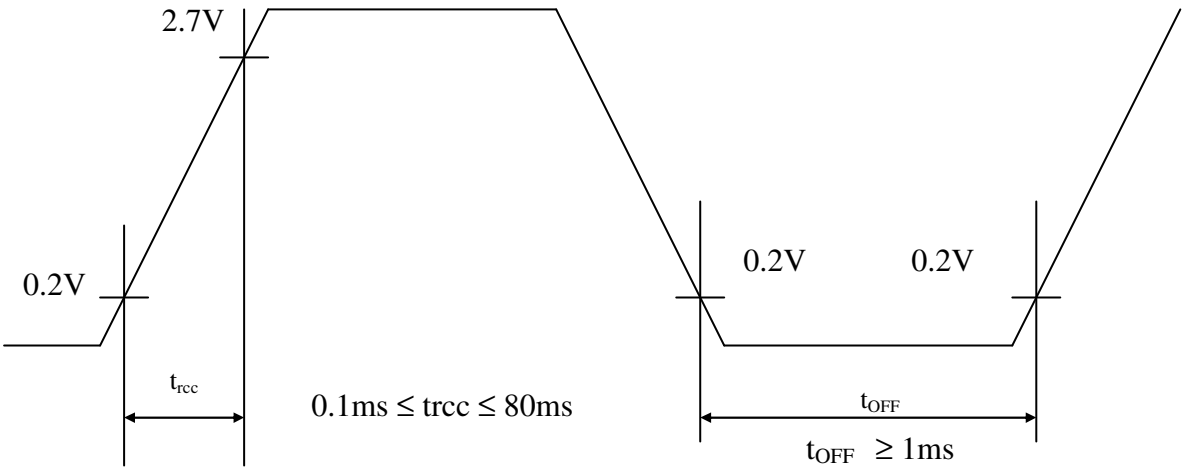
Writing data from MPU to SA8016 (Serial)



Reading data from SA8016 to MPU (Parallel)



Internal Power Supply Reset



Notes:

- t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
- Specified at 2.7V for 3V operation.
- For if 2.7V is not reached during 3V operation, the internal reset circuit will not operate normally.

AC Characteristics

In 6800 interface (Ta = 25C, VDD = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal clock operation						
f_{OSC}	OSC frequency	R= 150kΩ	250	330	410	kHz
External clock operation						
f_{EX}	External frequency	-	185	330	470	kHz
	Duty Cycle	-	45	50	55	%
t_r t_f	Rise / Fall time	-	-	-	0.2	μs
Write mode (Writing data from MPU to SA8016)						
t_{CYC}	Enable cycle time	Pin E (except clear display)	60	-	-	μs
t_{PW}	Enable pulse width	Pin E	30	-	-	ns
t_r t_f	Enable Rise / Fall time	Pin E	-	-	25	ns
t_{AS}	Address setup time	Pins: RS, RW, E	0	-	-	ns
t_{AH}	Address hold time	Pins: RS, RW, E	10	-	-	ns
t_{DS}	Data setup time	Pins: DB0 to DB7	30	-	-	ns
t_{DH}	Data hold time	Pins: DB0 to DB7	10	-	-	ns
Read mode (Reading data from SA8016 to MPU)						
t_{CYC}	Enable cycle time	Pin E	1200	-	-	ns
t_{PW}	Enable pulse width	Pin E	480	-	-	ns
t_r t_f	Enable Rise / Fall time	Pin E	-	-	25	ns
t_{AS}	Address setup time	Pins: RS, RW, E	0	-	-	ns
t_{AH}	Address hold time	Pins: RS, RW, E	10	-	-	ns
t_{OD}	Output delay time	Pins: DB0 to DB7	-	-	420	ns
t_{OH}	Output hold time	Pins: DB0 to DB7	10	-	-	ns

AC Characteristics

In Serial interface (Ta = 25C, VDD = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal clock operation						
f_{OSC}	OSC frequency	R= 150kΩ	250	330	410	kHz
External clock operation						
f_{EX}	External frequency	-	185	330	470	kHz
	Duty Cycle	-	45	50	55	%
t_r, t_f	Rise / Fall time	-	-	-	0.2	μs
Write mode (Writing data from MPU to SA8016)						
t_{SCYC}	SCLK cycle time	SCLK	2500	-	-	ns
t_{SHW}, t_{SLW}	SCLK pulse width	SCLK	1200	-	-	ns
t_r , t_f	SCLK Rise / Fall time	SCLK	-	-	25	ns
t_{SAS}	Address setup time	RS	75	-	-	ns
t_{SAH}	Address hold time	RS	10	-	-	ns
t_{SDS}	Data setup time	SID	10	-	-	ns
t_{SDH}	Data hold time	SID	75	-	-	ns
t_{CSS}	CS-SCLK time	CS	75	-	-	ns
t_{CSH}	CS-SCLK time	CS	250	-	-	ns

Absolute Maximum Ratings

Characteristics	Symbol	Value
Power supply voltage	V_{DD}	-0.3 to +5.5
LCD driver voltage	V_{LCD}	VSS+5.0 to VSS-0.3
Input voltage	V_{IN}	-0.3 to VDD+0.3
Operating temperature	Ta	-40C to +90C
Storage temperature	T_{STO}	-55C to +125C

DC Characteristics

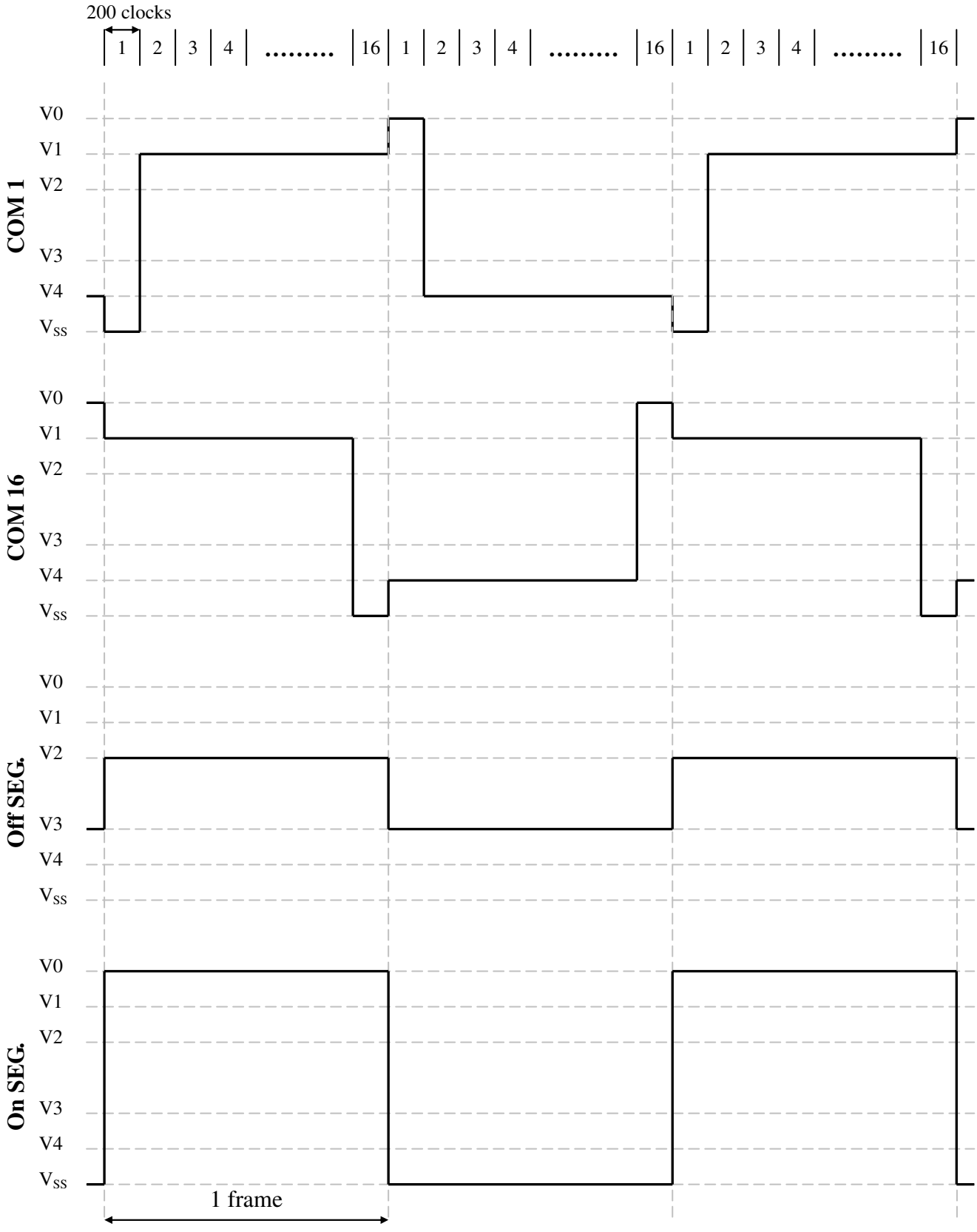
(Ta = 25C, V_{DD} = 2.7V – 3.5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	-	2.7	-	3.5	V
V_{LCD}	LCD voltage (unload)	V_{LCD}-V_{SS}	-	5.4	-	V
V_0	LCD voltage	V_0-V_{SS}	3.0	-	5.0	V
I_{DD}	Power supply current	fosc = 330kHz V_{DD} = 3.0V	-	0.2	0.4	mA
I_{DD}	Current with booster	V_{DD} = 3.0V	-	0.3	0.6	mA
V_{IH1}	Input High voltage (Except OSC1)	-	0.7V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low voltage (Except OSC1)	-	-0.3	-	0.6	V
V_{IH2}	Input High voltage (OSC1)	-	0.7V_{DD}	-	V_{DD}	V
V_{IL2}	Input Low voltage (OSC1)	-	-	-	0.2V_{DD}	V
V_{OH1}	Output High voltage (DB0 to DB7)	I_{OH} = -0.1mA	0.75V_{DD}	-	-	V
V_{OL1}	Output Low voltage (DB0 to DB7)	I_{OL} = 0.1mA	-	-	0.2V_{DD}	V
V_{OH2}	Output High voltage (Except DB0 to DB7)	I_{OH} = -0.04mA	0.8V_{DD}	-	V_{DD}	V
V_{OL2}	Output Low voltage (Except DB0 to DB7)	I_{OL} = 0.04mA	-	-	0.2V_{DD}	V
R_{COM}	Common Resistance	VLCD = 4V, Id = 0.05mA	-	2	20	kΩ
R_{SEG}	Segment Resistance	VLCD = 4V, Id = 0.05mA	-	2	30	kΩ
I_{LEAK}	Input leakage current	V_{IN} = 0V to V_{DD}	-1	-	1	µA
I_{PUP}	Pull up MOS current	V_{DD} = 3V	20	60	120	µA

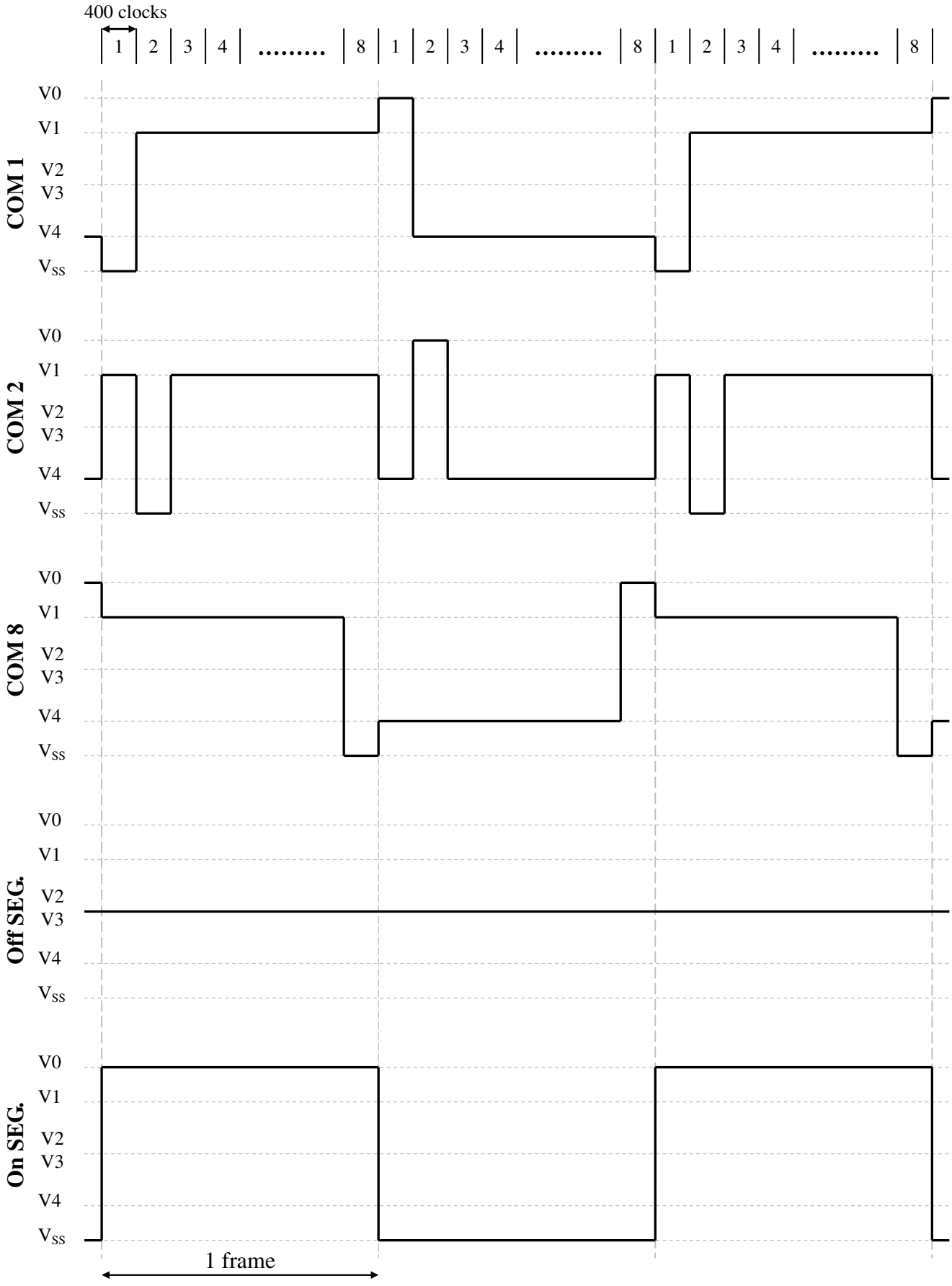
Note: External bias resistor select, so Idd doesn't include the follower current.

LCD Frame frequency

Assume the oscillation frequency is 270kHz, 1 clock cycle time = 3.7µs, 1/16 duty; 1/5 bias, 1 frame = 3.7µs x 200 x 16 = 11840µs = 11.8ms (84.7Hz)

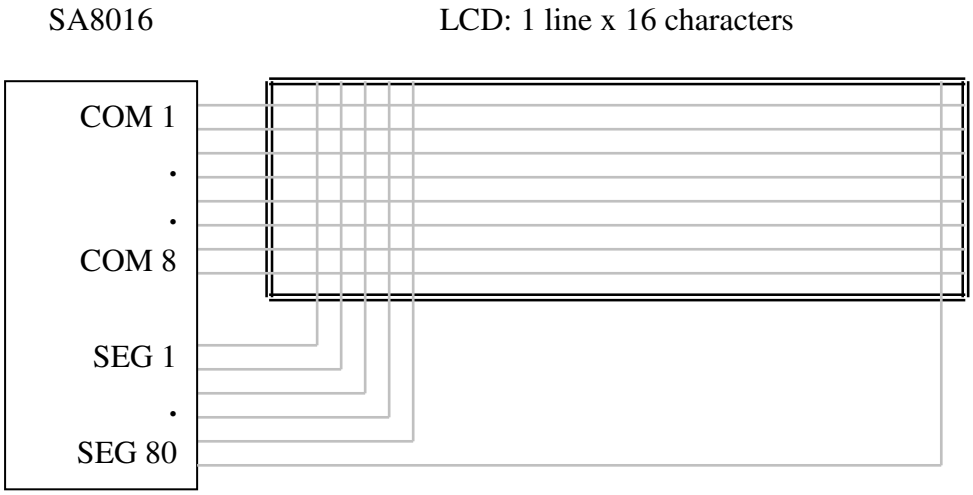


Assume the oscillation is 270kHz, 1 clock cycle time = 3.7µs, 1/8 duty; 1/4 bias, 1 frame = 3.7µs x 400 x 8 = 11840µs = 11.8ms (84.7Hz)

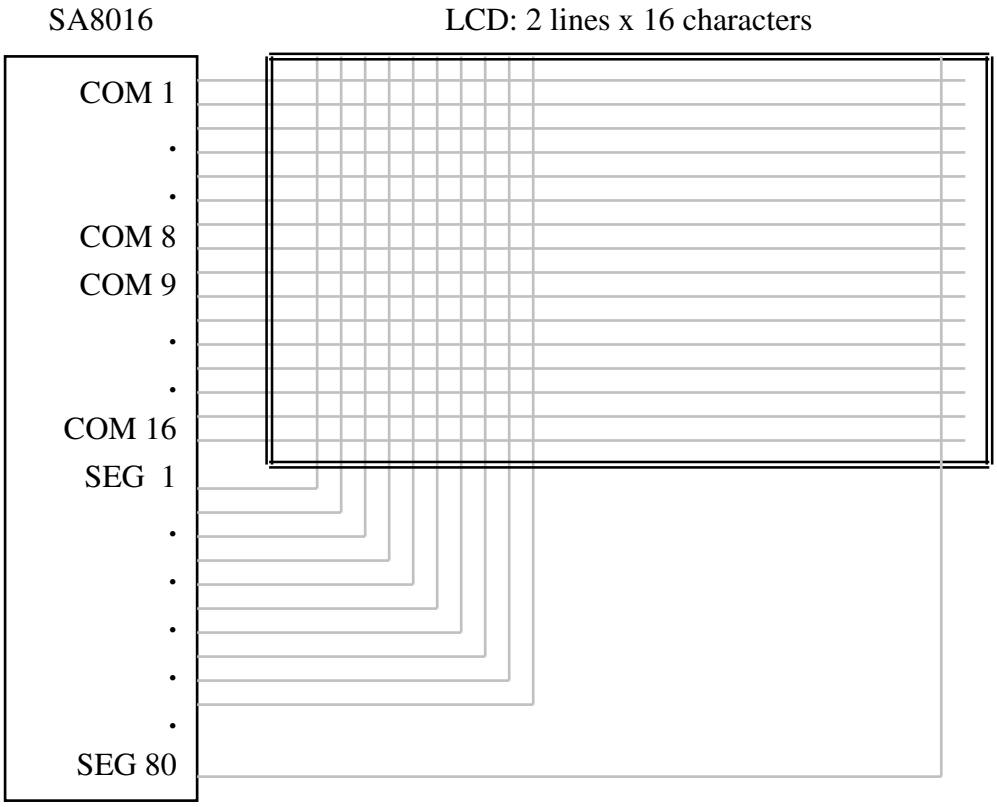


LCD and SA8016 connection

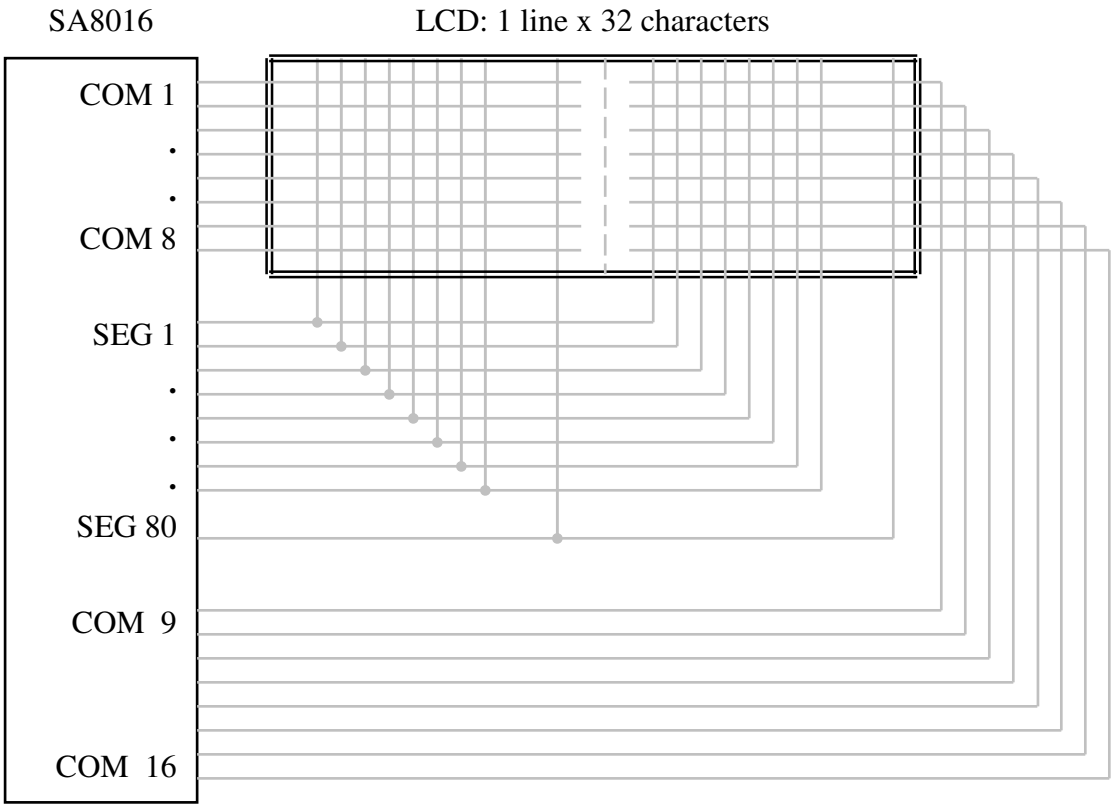
1. 5x8 dots, 1 line x 16 characters (1/4 bias, 1/8 duty)



2. 5x8 dots, 2 line x 16 characters (1/5 bias, 1/16 duty)



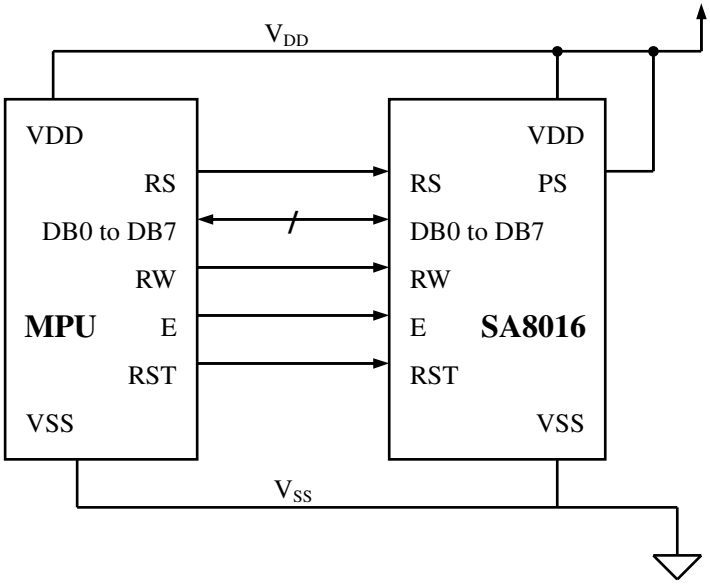
3. 5x8 dots, 1 line x 32 characters (1/5 bias, 1/16 duty)



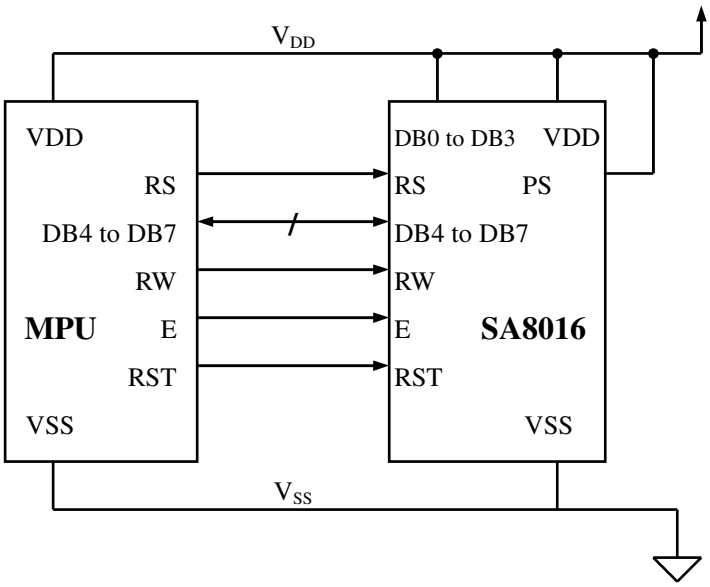
The MPU interface

SA8016 can be connected to 6800 series MPU. Moreover using the serial interface it is possible to operate the SA8016 chip with fewer signal lines.
Using multiple SA8016 can enlarge the display area. When this is done, the chip select signal can be used to select the individual to access.

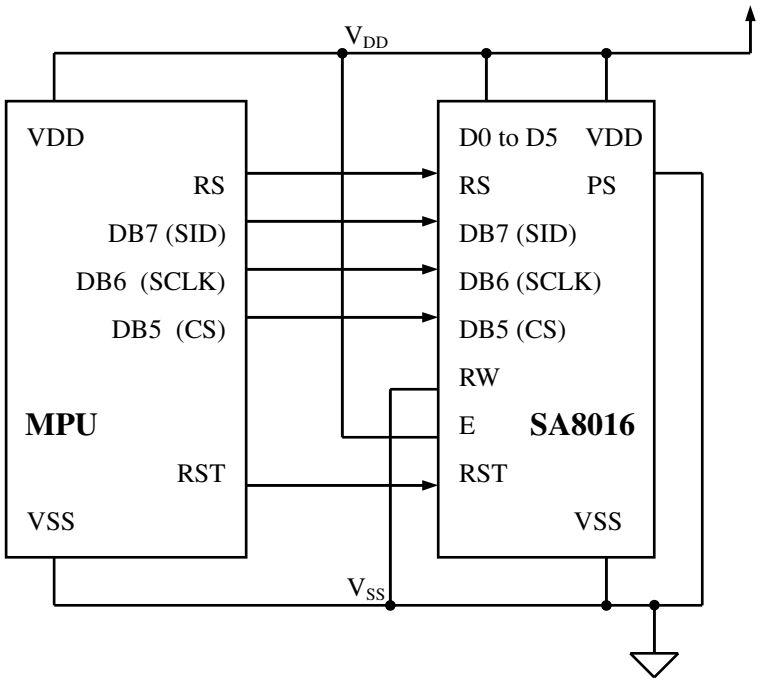
1. 6800 8 bit series MPU



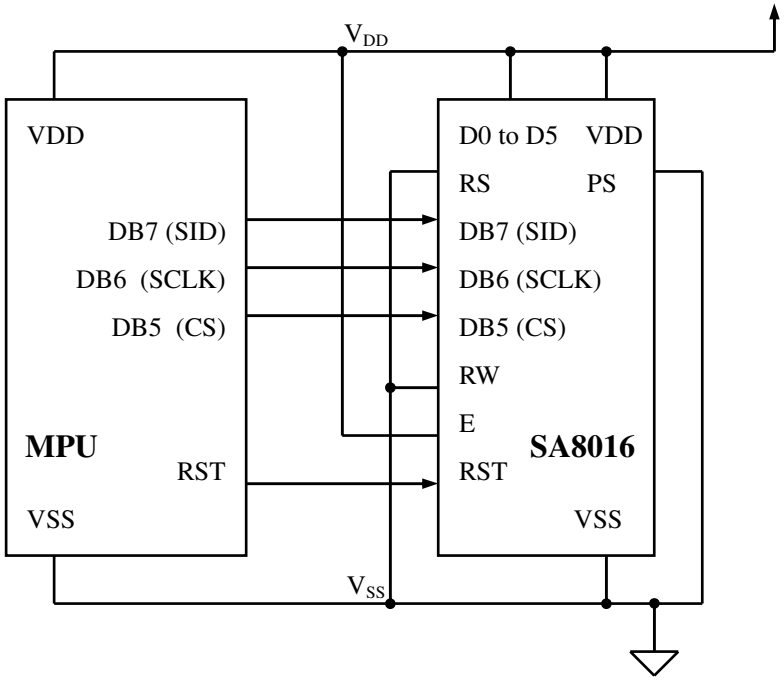
2. 6800 4 bit series MPU



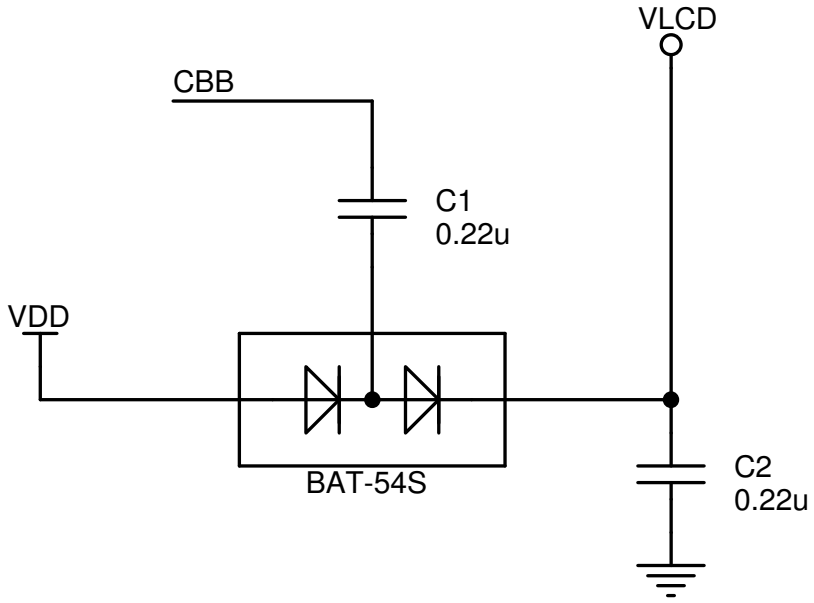
3. 4 pin SPI serial interface



4. 3 pin SPI serial interface



Circuit for the charge bump of SA8016 CBB pin



Note:

The CBB pin output the charge bump of signal to capacitor and diode to charge up the VDD to the VLCD.

Diode recommends using BAT54 series or Schottky diode.

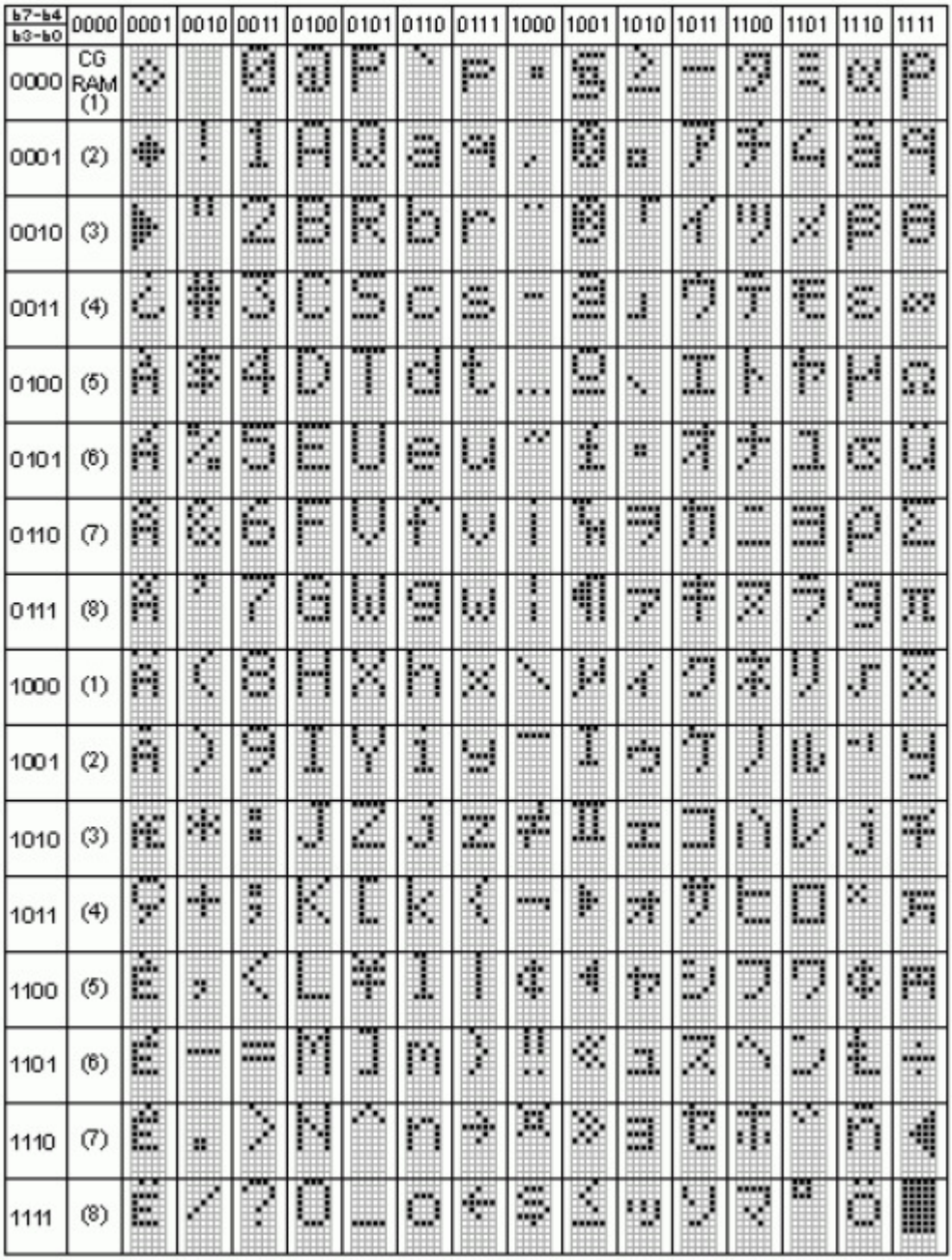
Typically, charge pump circuit performance is about 80%

VLCD = VDD * 1.8

Therefore,

VDD = 3V, VLCD = 5.4V

Font table for Character Codes and Character Patterns (Page 1)



Font table for Character Codes and Character Patterns (Page 2)